

DESIGN NOTES

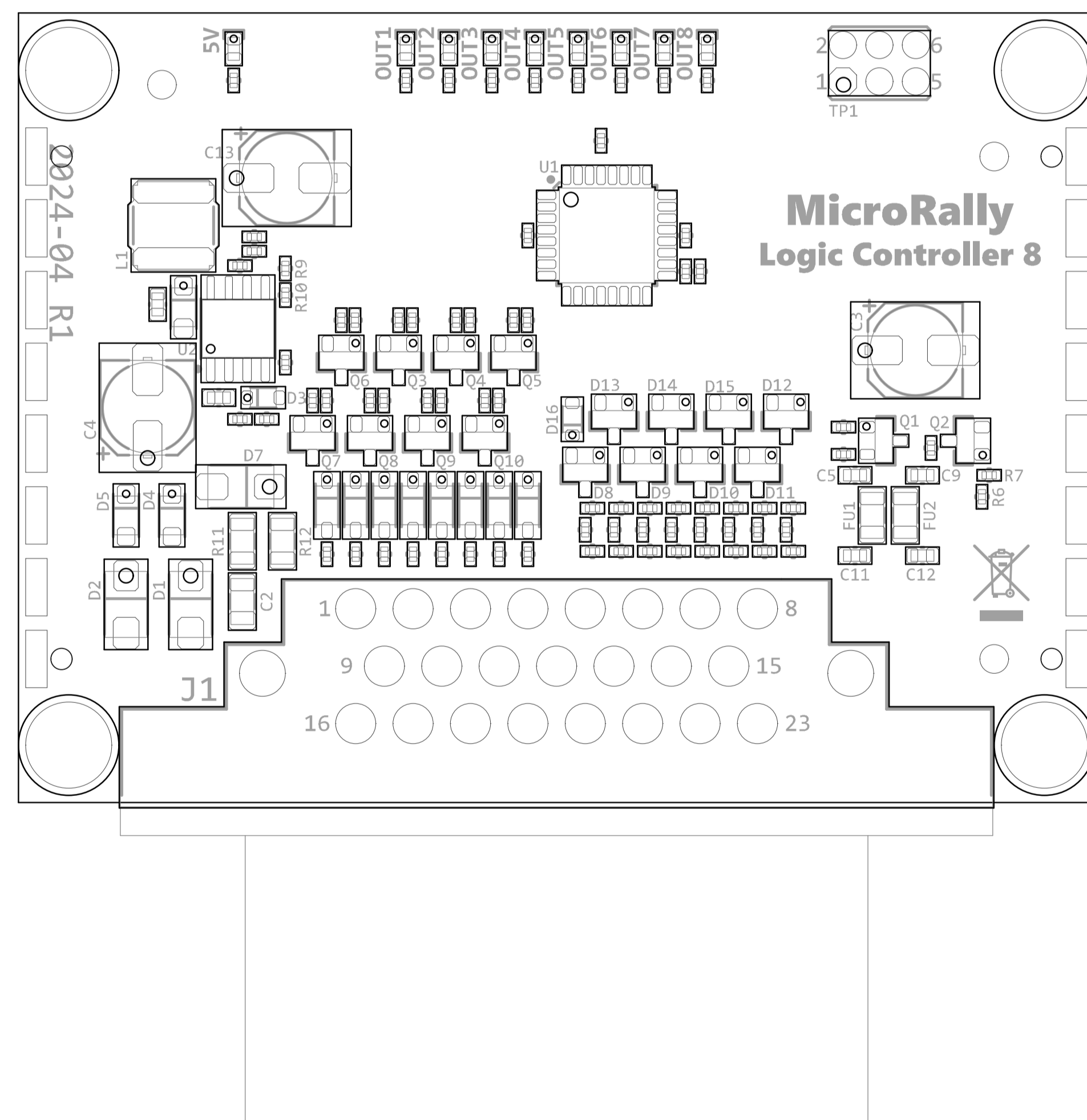
MAIN CONNECTOR

TE AMPSEAL 23 PIN RIGHT ANGLE (776087-x)

VBAT	OUT1	OUT2	OUT3	IN1	IN2	IN3	5V	
	IGN	OUT4	OUT5	GND	IN4	IN5	5VSW	
	GND	OUT6	OUT7	OUT8	IN6	IN7	IN8	GND

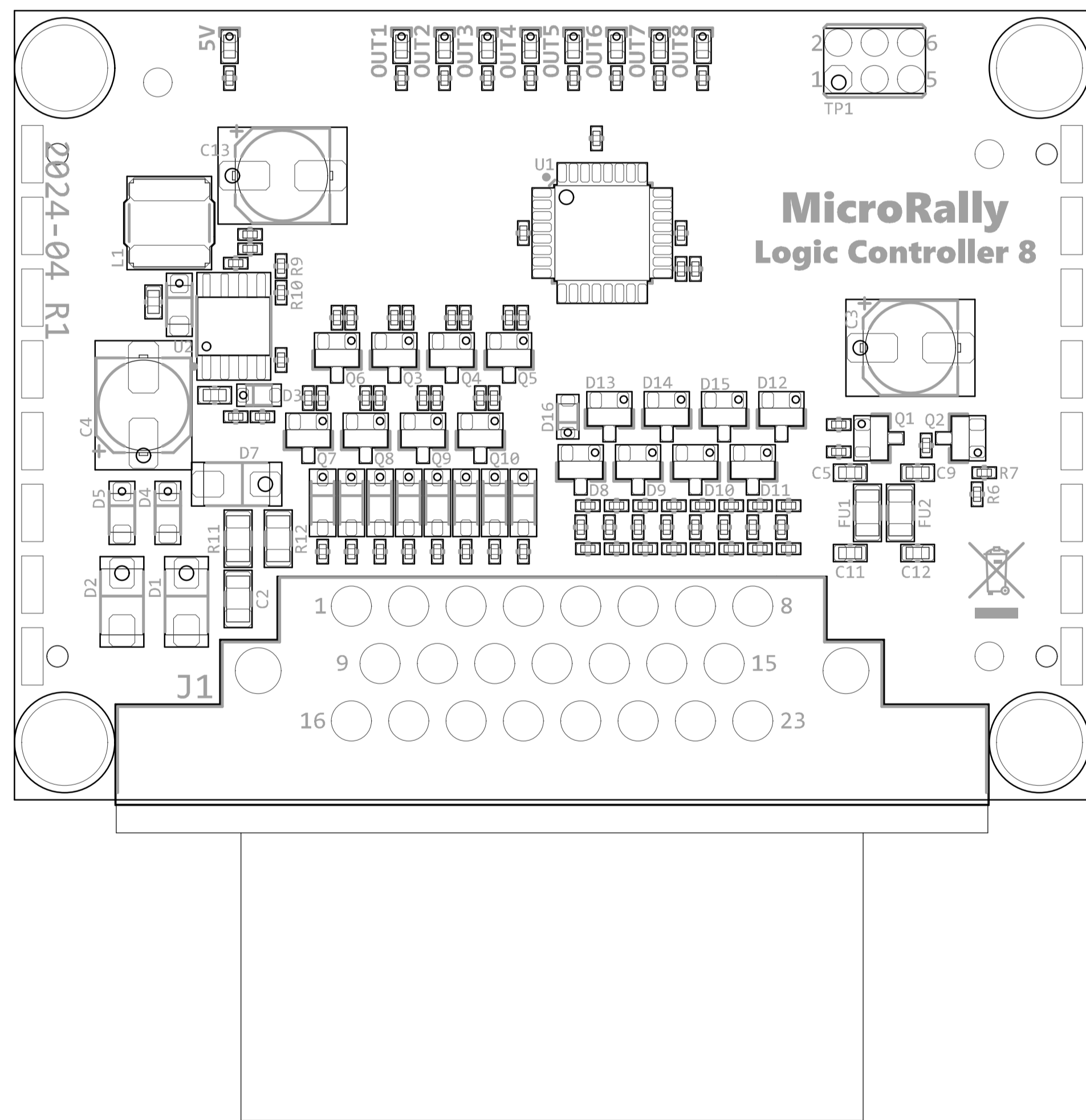
ISP HEADER

5V	MOSI	GND
MISO	SCK	RST

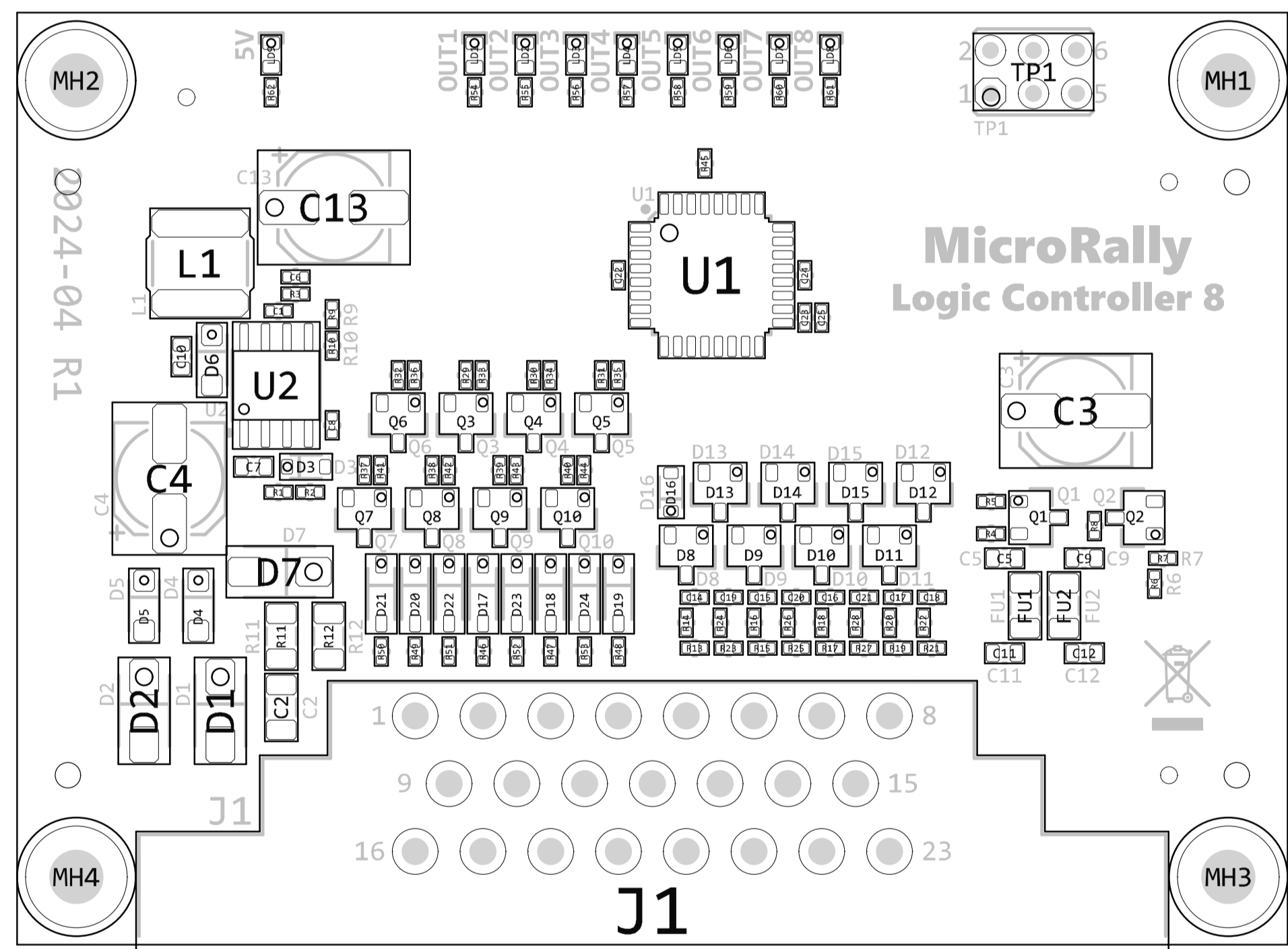


Title: PCB Drawing			MicroRally
Project: Logic Controller 8			
Revision: r1	Size: A4	Scale: 1:1	Engineer: Andis Zile
File: logic-controller.PcbDoc			Date: 24.04.2024

ASSEMBLY NOTES



Title: PCB Drawing			MicroRally
Project: Logic Controller 8			
Revision: r1	Size: A4	Scale: 1:1	Engineer: Andis Zile
File: logic-controller.PcbDoc			Date: 24.04.2024

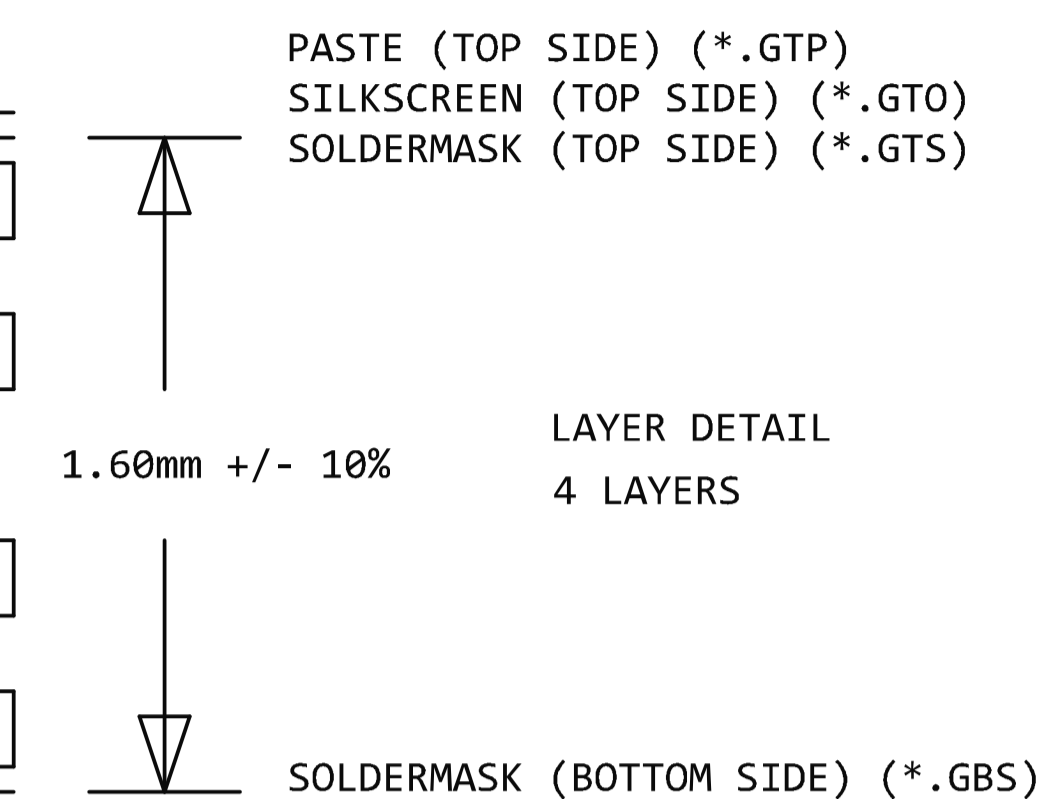
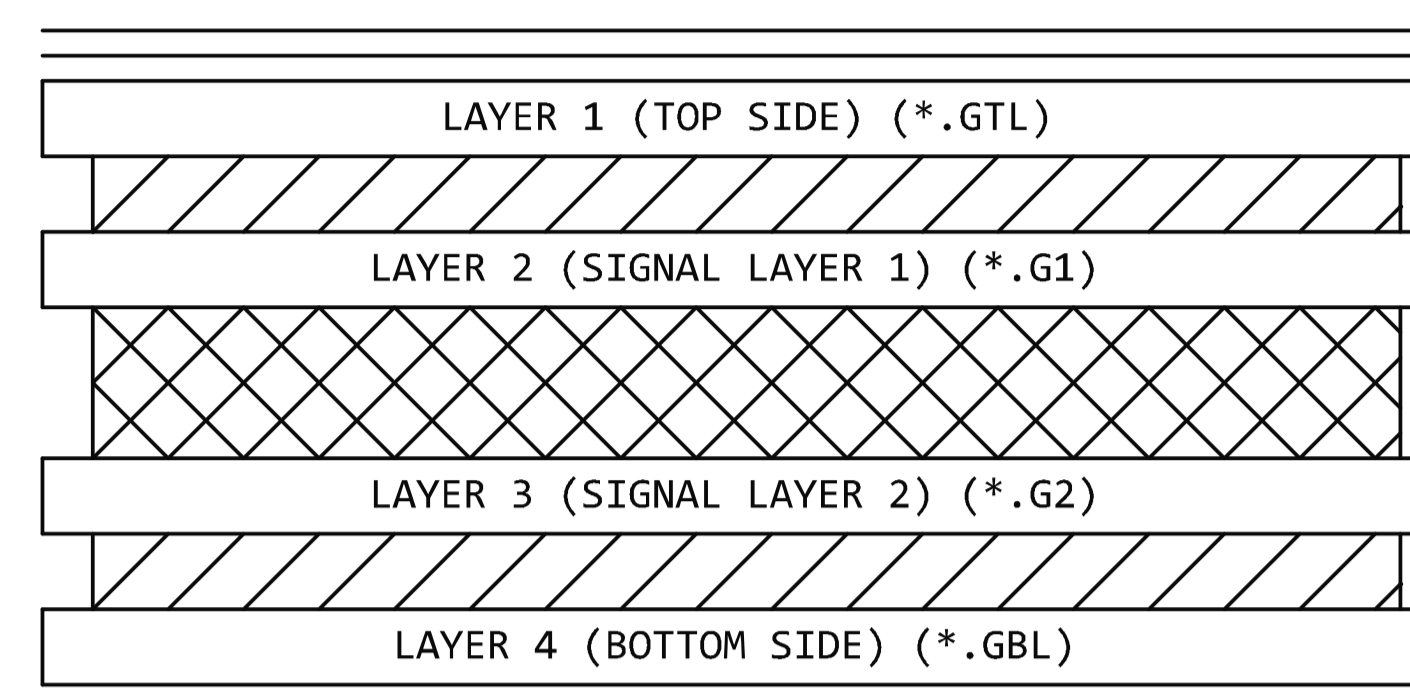


Title: PCB Drawing			MicroRally
Project: Logic Controller 8			
Revision: r1	Size: A4	Scale: 1:1	Engineer: Andis Zile
File: logic-controller.PcbDoc			Date: 24.04.2024

FABRICATION NOTES

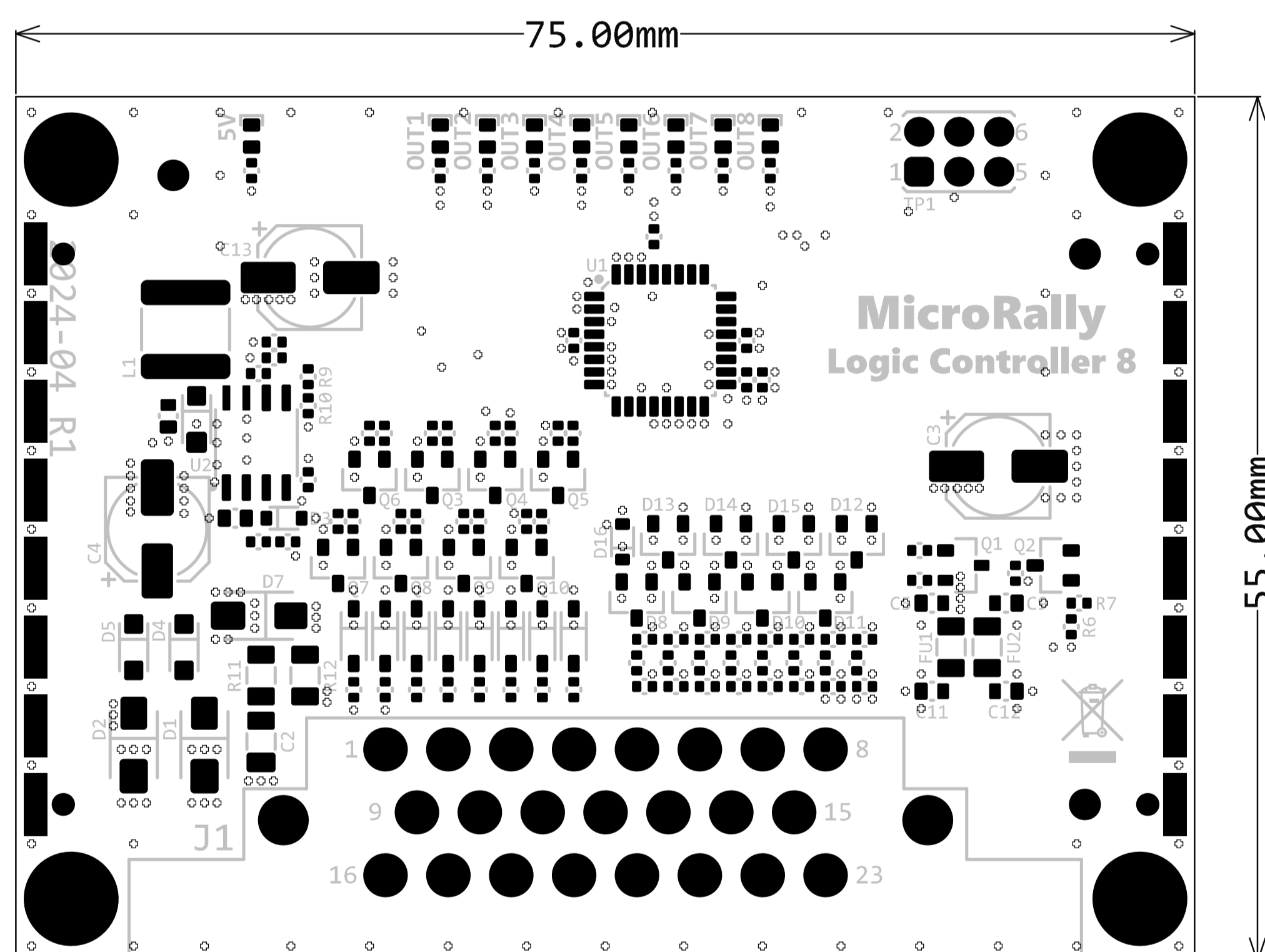
Symbol	Count	Hole Size	Plated	Hole Type	Via/Pad
⊕	27	0.30mm	PTH	Round	Via
▽	6	1.00mm	PTH	Round	Pad
□	4	1.15mm	NPTH	Round	Pad
⊛	23	1.60mm	PTH	Round	Pad
⊗	2	2.85mm	NPTH	Round	Pad
○	4	3.20mm	PTH	Round	Pad
	336 Total				

1.0 OZ L1
 0.2104 mm Prepreg 7628
 0.5 OZ L2
 1.050 mm Core - FR4
 0.5 OZ L3
 0.2104 mm Prepreg 7628
 1.0 OZ L4



NOTES:

- THIS IS 4 LAYER BOARD
- MATERIAL: FR4, TG 150 DEGREE C MIN
- FR4 DIELECTRIC CONSTANT NOT SPECIFIED
- FINISHED BOARD THICKNESS TO BE 1.60MM +/- 10%
- TRACE WIDTHS IN ARTWORK ARE FINISHED SIZES
- SEE FILM FOR LAYER SEQUENCE AND COPPER THICKNESSES (SHOWN AFTER PLATING)
- MIN TRACE/SPACE 0.20/0.20 MM
- SEE DRILL CHART FOR FINISHED HOLE SIZES
- MIN DRILL 0.30MM
- MAX ALLOWABLE BOW AND TWIST FOR COMPLETE PANEL 0.75%
- SURFACE PLATING: LEAD FREE HASL
- SOLDERMASK: LPI, BOTH SIDES. COLOR GREEN
- SILKSCREEN: TOP AND BOTTOM SIDE. COLOR WHITE
- FABRICATE PER THE LATEST REVISION OF IPC-6012 (IPC-6018 FOR HDI BOARDS) CLASS 2
- BOARDS MUST COMPLY WITH UL 94V-0.
- MFR UL LOGO, UL MARKING, DATE CODE (YYWW), AND LAMINATE PART NUMBER TO BE PLACED IN SILKSCREEN ON TOP SIDE
- BOARDS MUST COMPLY WITH THE LATEST REVISION OF THE ROHS DIRECTIVE
- ALL BOARDS MUST BE ELECTRICALLY TESTED FOR ISOLATION (SHORTS) AND CONTINUITY (OPENS)
- COMPLETE BOARDS TO BE HANDLED AND PACKED AS PER IPC-1601
- SPECIFY USED LAMINATE SHEET SIZE AND UTILIZATION PERCENTAGE IN THE QUOTE SUBMITTED
- PRODUCTION (WORKING) GERBER FILES REQUIRE PRIOR MANUFACTURING APPROVAL FROM THE DESIGNER
- THIEVING NOT ALLOWED
- ANY CHANGES TO THE STACK-UP AND DK VALUE SPECIFIED MUST BE APPROVED BY THE DESIGNER



Title: PCB Drawing			MicroRally
Project: Logic Controller 8			
Revision: r1	Size: A4	Scale: 1:1	Engineer: Andis Zile
File: logic-controller.PcbDoc			Date: 24.04.2024

1

2

3

4

A

A

B

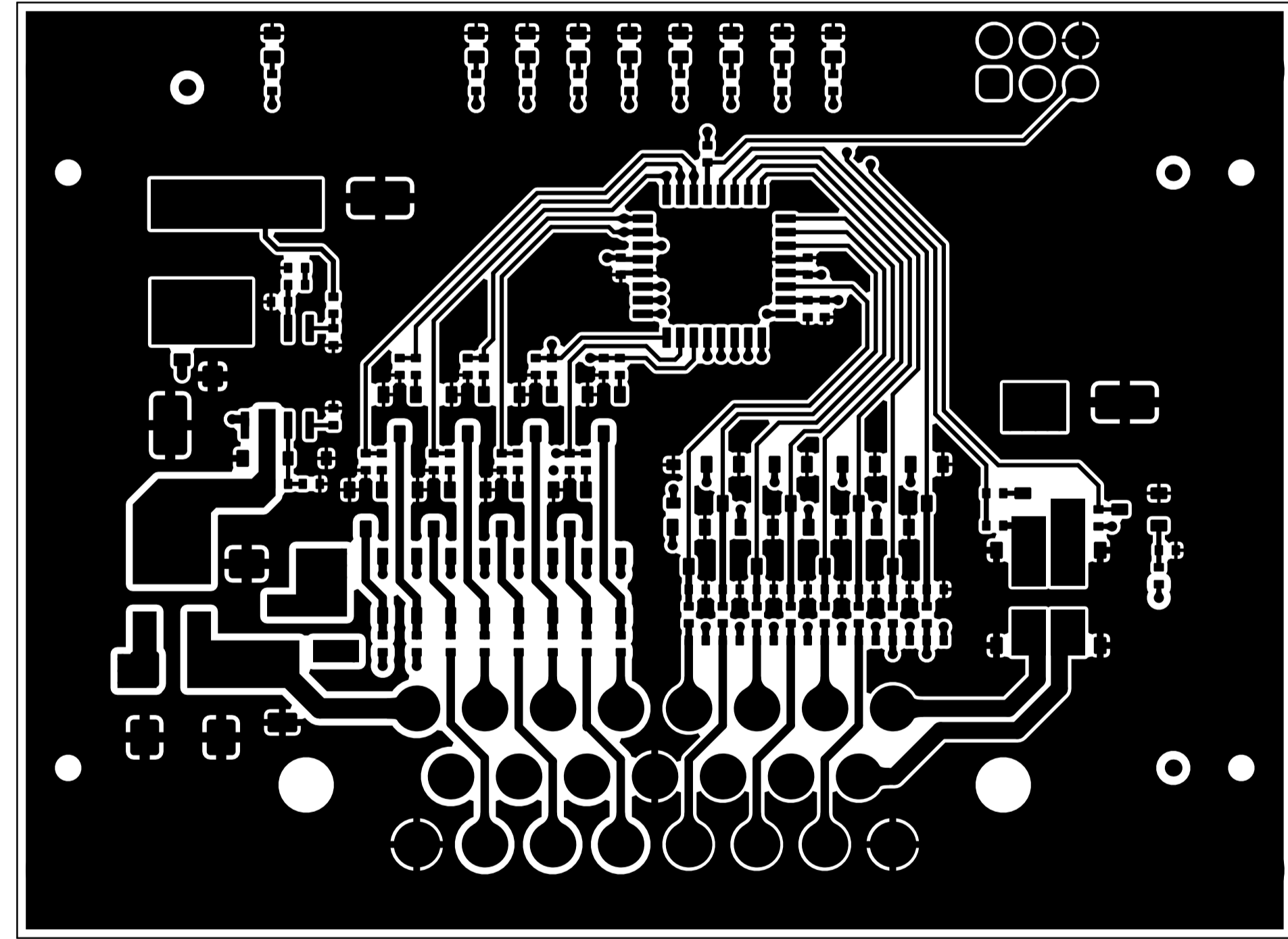
B

C

C

D

D



Title: PCB Drawing			MicroRally
Project: Logic Controller 8			
Revision: r1	Size: A4	Scale: 1:1	Engineer: Andis Zile
File: logic-controller.PcbDoc			Date: 24.04.2024

1

2

3

4

1

2

3

4

A

A

B

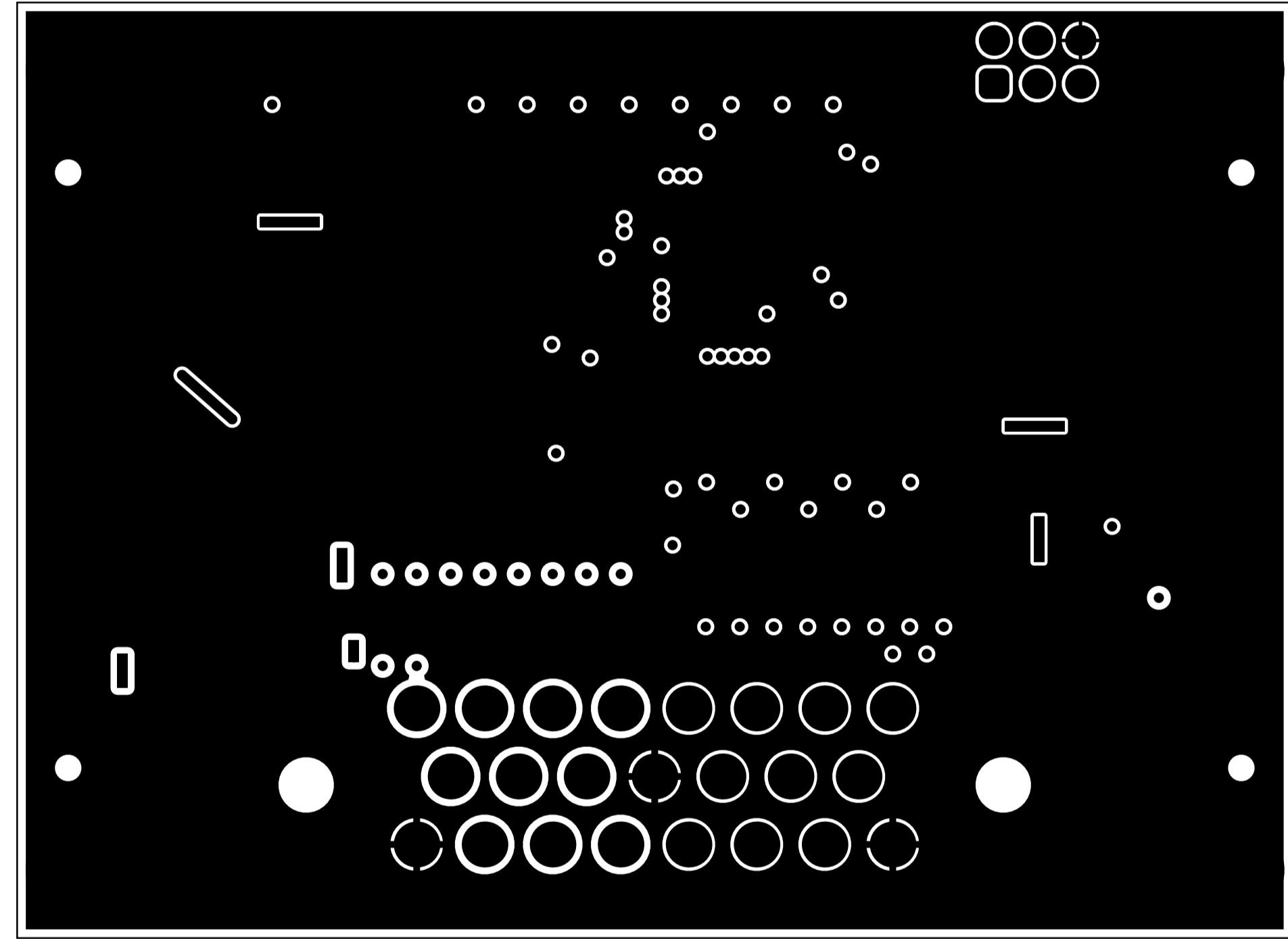
B

C

C

D

D



Title: PCB Drawing			MicroRally
Project: Logic Controller 8			
Revision: r1	Size: A4	Scale: 1:1	Engineer: Andis Zile
File: logic-controller.PcbDoc			Date: 24.04.2024

1

2

3

4

1

2

3

4

A

A

B

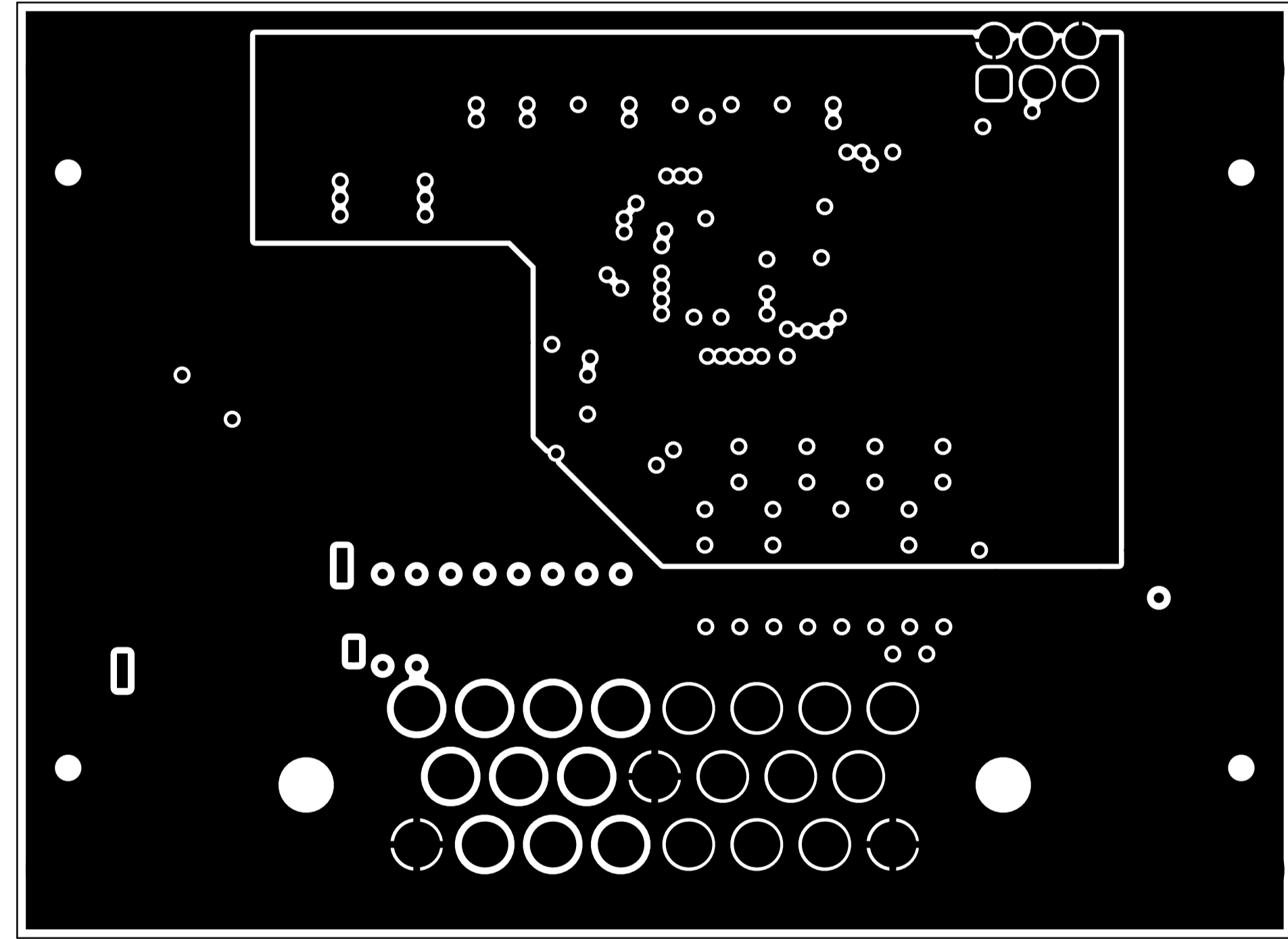
B

C

C

D

D



Title: PCB Drawing			MicroRally
Project: Logic Controller 8			
Revision: r1	Size: A4	Scale: 1:1	Engineer: Andis Zile
File: logic-controller.PcbDoc			Date: 24.04.2024

1

2

3

4

1

2

3

4

A

A

B

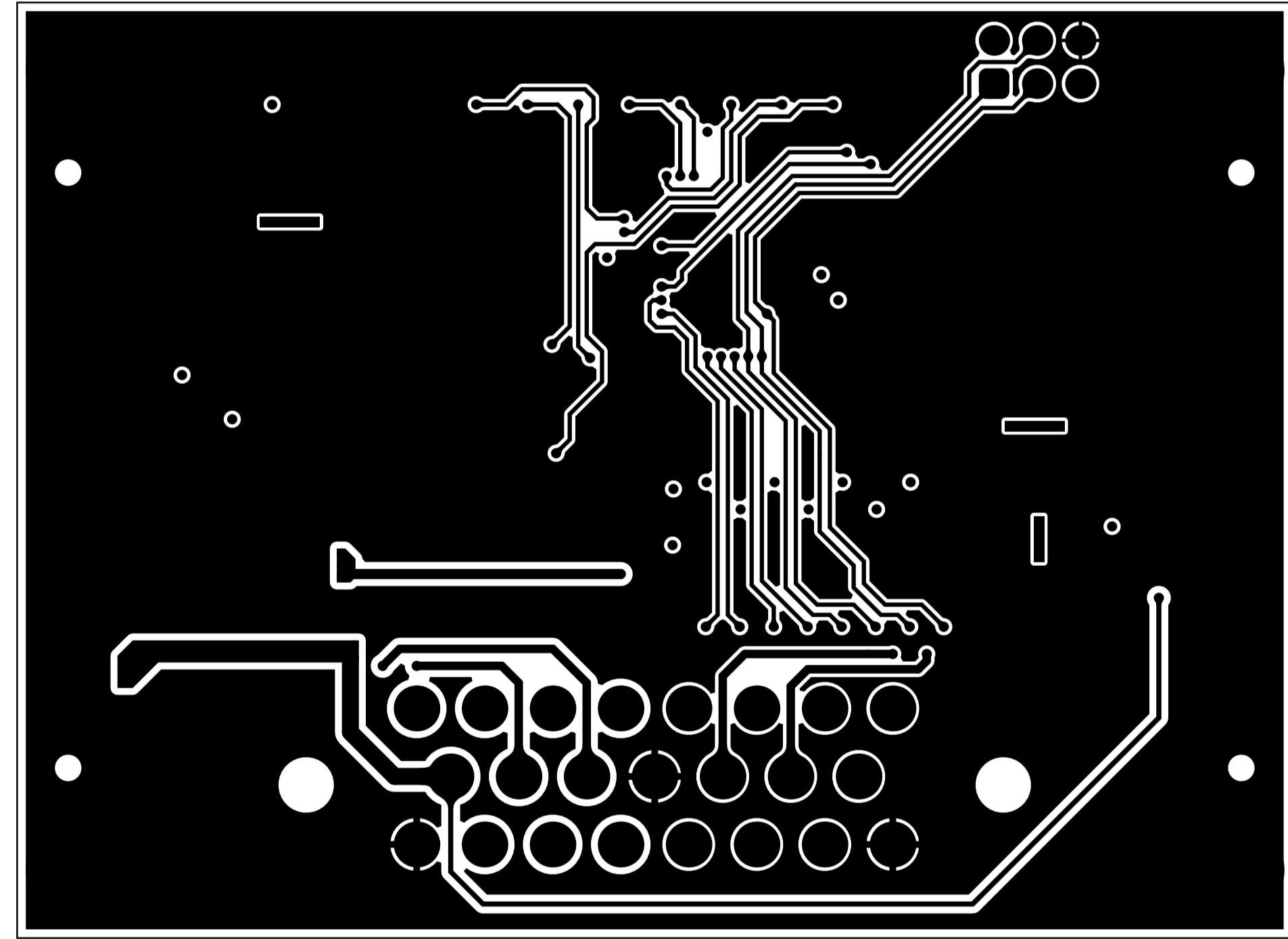
B

C

C

D

D



Title: PCB Drawing			MicroRally
Project: Logic Controller 8			
Revision: r1	Size: A4	Scale: 1:1	Engineer: Andis Zile
File: logic-controller.PcbDoc			Date: 24.04.2024

1

2

3

4

