

MicroRally

Logic Controller 8

8 channel logic controller with 5V analog inputs and open-drain outputs

PCB Revision r1

Title: Cover page				MicroRally
Project: Logic Controller 8				
PCB: r1	BOM: v1	Sheet 1 of 10	Size: A4	Engineer: Andis Zile
File: cover_page.SchDoc				Date: 24.04.2024

Index

Page	Title
1	Cover page
2	Index
3	Block Diagram
4	Connector
5	Power
6	Inputs
7	Outputs
8	Controller
9	Miscellaneous
10	Revision History

A

A

B

B

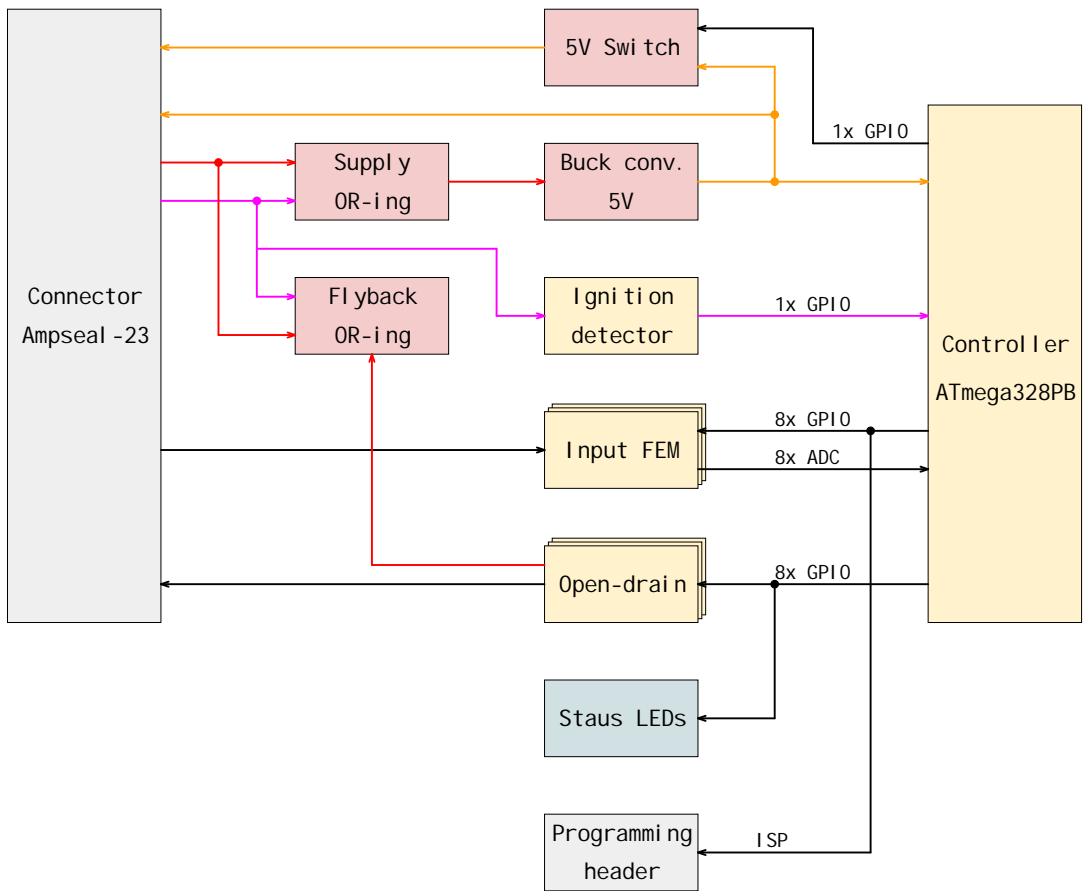
C

C

D

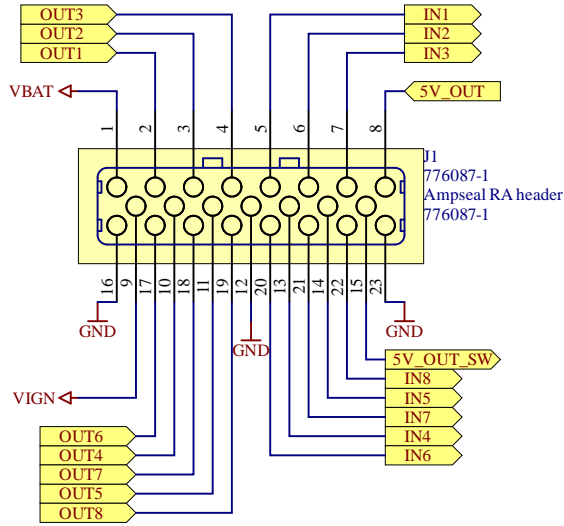
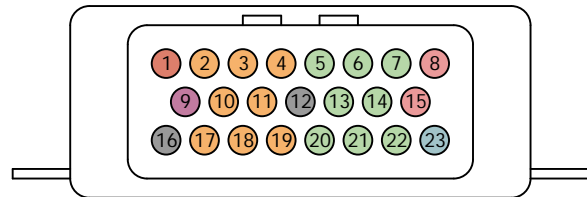
D

Title: Index				MicroRally
Project: Logic Controller 8				
PCB: r1	BOM: v1	Sheet 2 of 10	Size: A4	Engineer: Andis Zile
File: index.SchDoc				Date: 24.04.2024



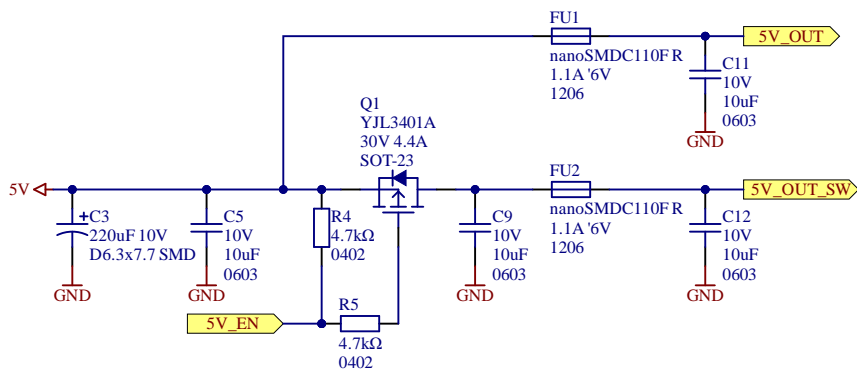
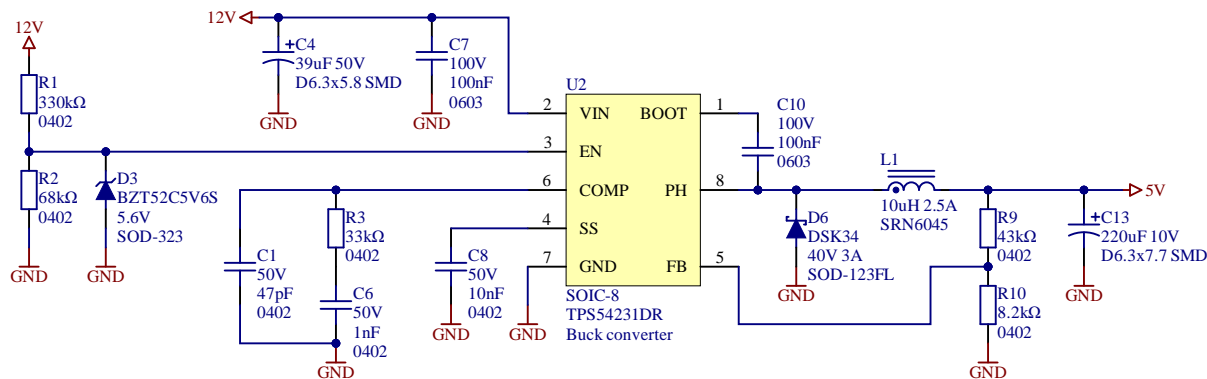
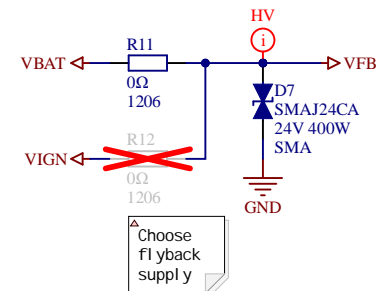
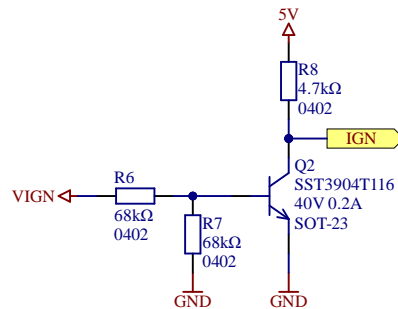
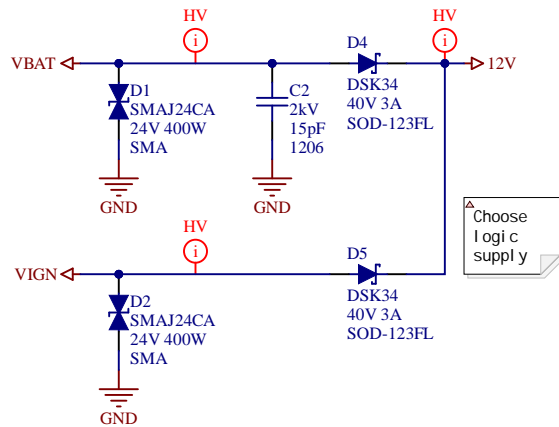
Title: Block diagram				MicroRally
Project: Logic Controller 8				
PCB: r1	BOM: v1	Sheet 3 of 10	Size: A4	Engineer: Andis Zile
File: block_diagram.SchDoc				Date: 24.04.2024

MAIN CONNECTOR

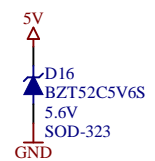
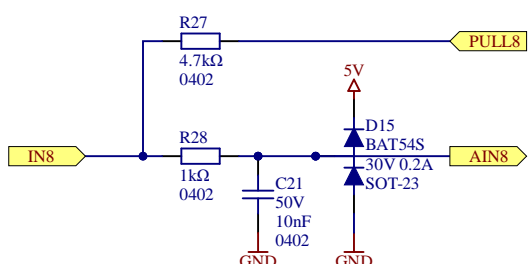
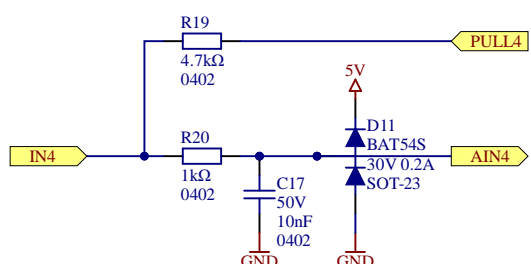
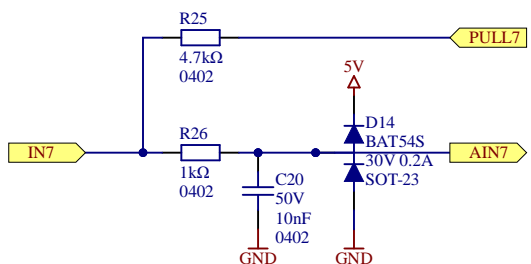
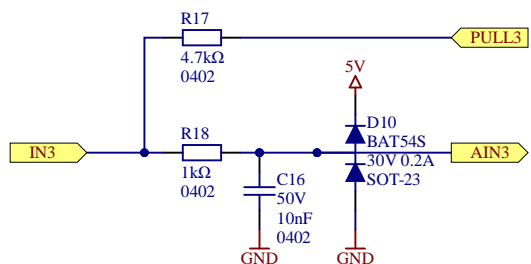
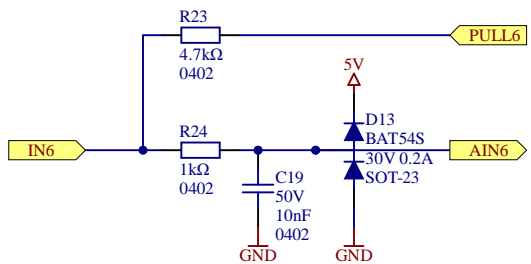
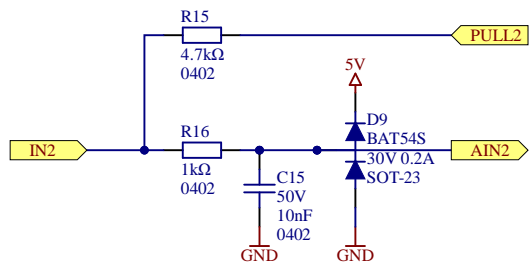
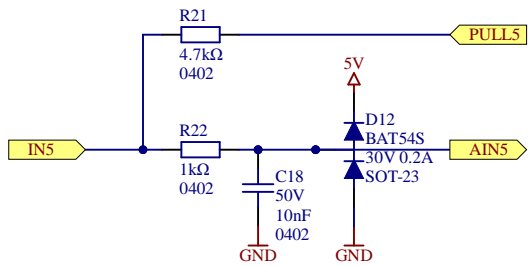
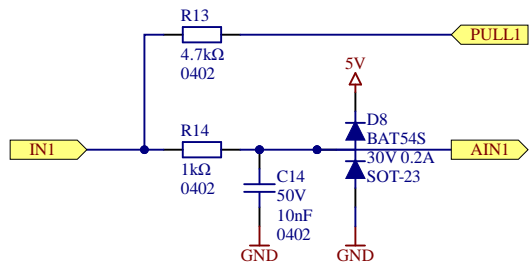


1	VBAT	Battery power input
2	OUT1	Open-drain output
3	OUT2	Open-drain output
4	OUT3	Open-drain output
5	IN1	Analog input
6	IN2	Analog input
7	IN3	Analog input
8	5V	5V supply output
9	IGN	Ignition power
10	OUT4	Open-drain output
11	OUT5	Open-drain output
12	OD1	Outputs ground
13	IN4	Analog input
14	IN5	Analog input
15	5V SW	Switched 5V output
16	GND	Power ground
17	OUT6	Open-drain output
18	OUT7	Open-drain output
19	OUT8	Open-drain output
20	IN6	Analog input
21	IN7	Analog input
22	IN8	Analog input
23	GND	Inputs ground

Title: Connector				MicroRally
Project: Logic Controller 8				
PCB: r1	BOM: v1	Sheet 4 of 10	Size: A4	Engineer: Andis Zile
File: connector.SchDoc				Date: 24.04.2024

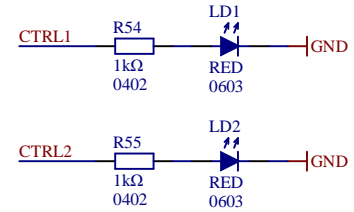
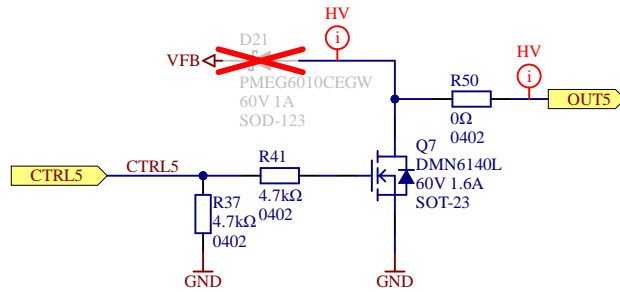
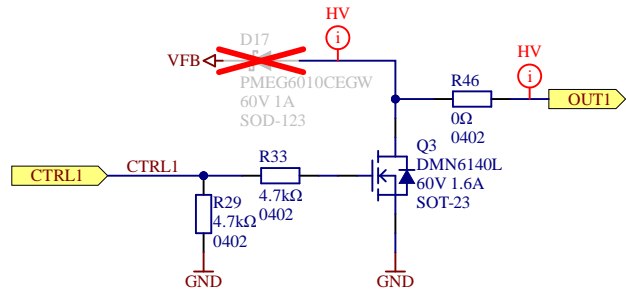


Title: Power				MicroRally
Project: Logic Controller 8				
PCB: r1	BOM: v1	Sheet 5 of 10	Size: A4	Engineer: Andis Zile
File: power.SchDoc				Date: 24.04.2024

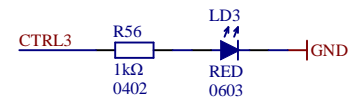
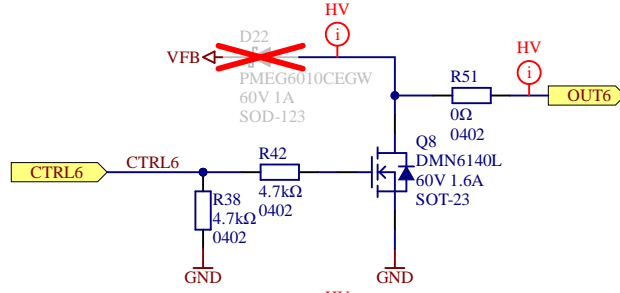
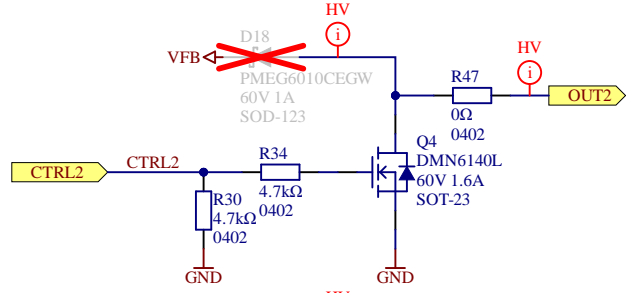


Title: Inputs				MicroRally
Project: Logic Controller 8				
PCB: r1	BOM: v1	Sheet 6 of 10	Size: A4	Engineer: Andis Zile
File: inputs.SchDoc				Date: 24.04.2024

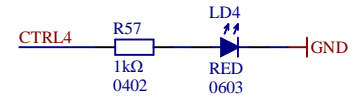
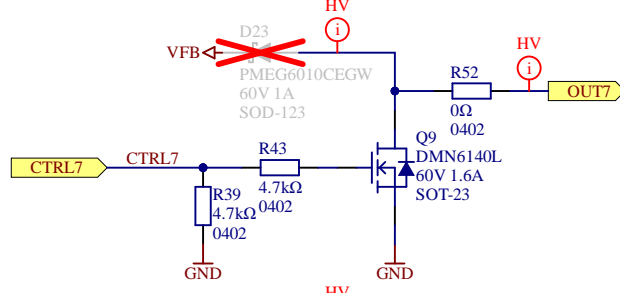
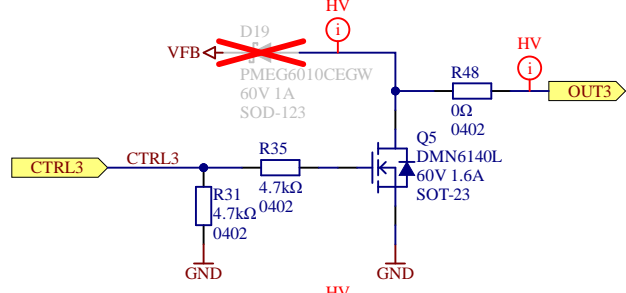
A



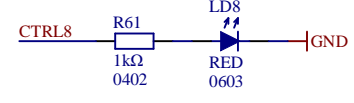
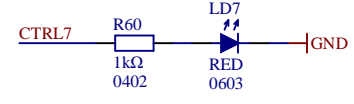
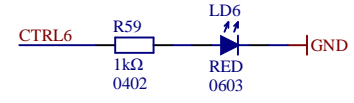
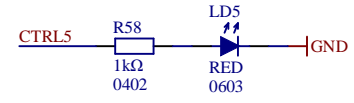
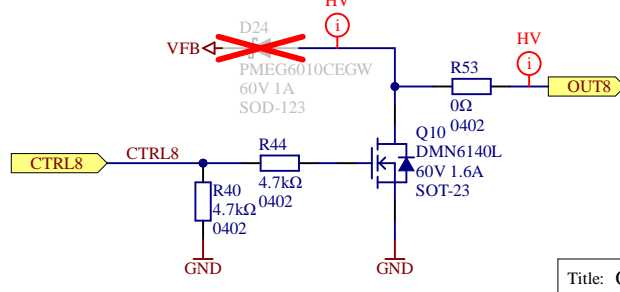
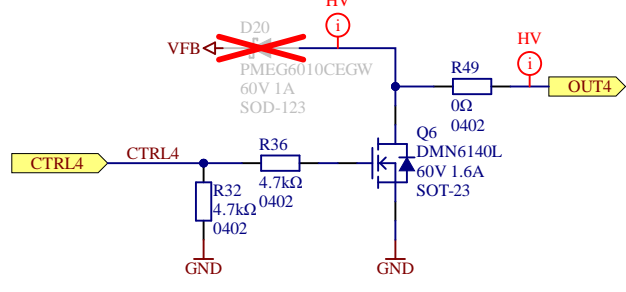
B



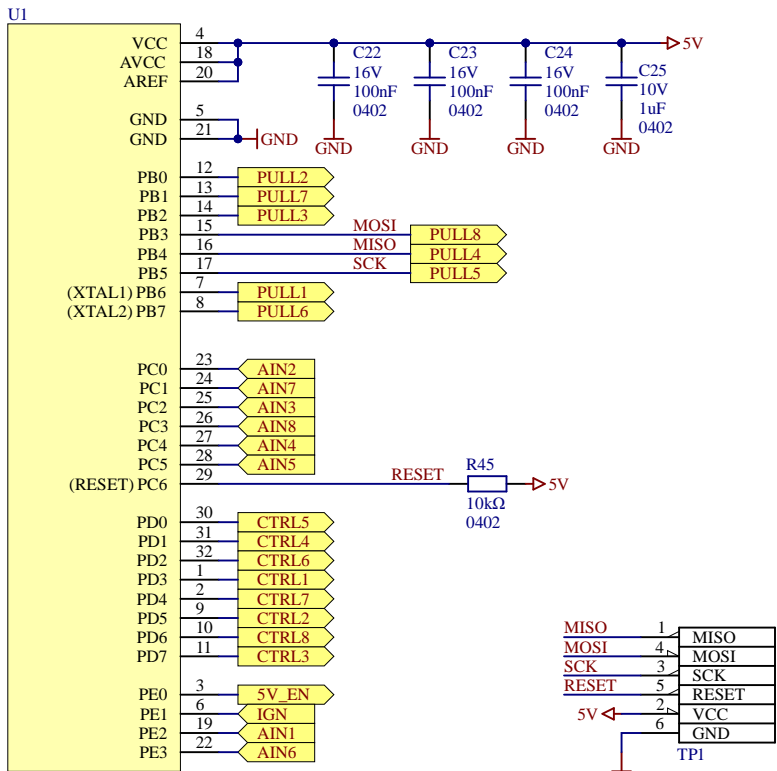
C



D



Title: Outputs				MicroRally
Project: Logic Controller 8				
PCB: r1	BOM: v1	Sheet 7 of 10	Size: A4	Engineer: Andis Zile
File: outputs.SchDoc				Date: 24.04.2024



ATMEGA328PB-AU
AVR 8bit
TQFP-32

#	Pin	GPIO	Special	Analog	Timer 0 (8b)	Timer 1	Timer 2 (8b)	Timer 3	Timer 4	UART	SPI	I2C	INT	Usage
12	PB0	OUT	CLKO			ICP1								Pull-2
13	PB1	OUT				OC1A								Pull-7
14	PB2	OUT				OC1B								Pull-3
15	PB3	OUT					OSC2A			TXD1	MOSI0			Pull-8 / ISP
16	PB4	OUT								RXD1	MISO0			Pull-4 / ISP
17	PB5	OUT								XCK1	SCK0			Pull-5 / ISP
7	PB6	OUT	XTAL1 / TOSC1											Pull-1
8	PB7	OUT	XTAL2 / TOSC2											Pull-6
23	PC0	IN		ADC0							MISO1			Input 2
24	PC1	IN		ADC1							SCK1			Input 7
25	PC2	IN		ADC2										Input 3
26	PC3	IN		ADC3										Input 8
27	PC4	IN		ADC4								SDA0		Input 4
28	PC5	IN		ADC5								SCL0		Input 5
29	PC6		RESET											ISP
30	PD0	OUT						OC3A		RXD0				Output 5
31	PD1	OUT							OC4A	TXD0				Output 4
32	PD2	OUT						OC3B	OC4B				INT0	Output 6
1	PD3	OUT						OC2B					INT1	Output 1
2	PD4	OUT			T0					XCK0				Output 7
9	PD5	OUT			OC0B	T1								Output 2
10	PD6	OUT		AIN0	OC0A									Output 8
11	PD7	OUT		AIN1										Output 3
3	PE0			ACO						ICP4		SDA1		Ignition
6	PE1								T4			SCL1		5V Enable
19	PE2	IN		ADC6				ICP3			SS1			Input 1
22	PE3	IN		ADC7				T3			MOSI1			Input 6

Title: Controller				MicroRally
Project: Logic Controller 8				
PCB: r1	BOM: v1	Sheet 8 of 10	Size: A4	Engineer: Andis Zile
File: mcu.SchDoc				Date: 24.04.2024

PCB Sheet

H1

Stackup note

H3

Gerber Notes 1.0

H4

WEEE

H2



F11



F12



F13



TH1



TH2



TH3



TH4

MH1



MH2



MH3



MH4



Title: Miscellaneous				MicroRally
Project: Logic Controller 8				
PCB: r1	BOM: v1	Sheet 9 of 10	Size: A4	Engineer: Andis Zile
File: miscellaneous.SchDoc				Date: 24.04.2024

Revision history

PCB	BOM	Date	Fixed issue	Changes
R1	V1	2024-04-24		Initial design

Title: Revision history				MicroRally
Project: Logic Controller 8				
PCB: r1	BOM: v1	Sheet 10 of 10	Size: A4	Engineer: Andis Zile
File: history.SchDoc				Date: 24.04.2024