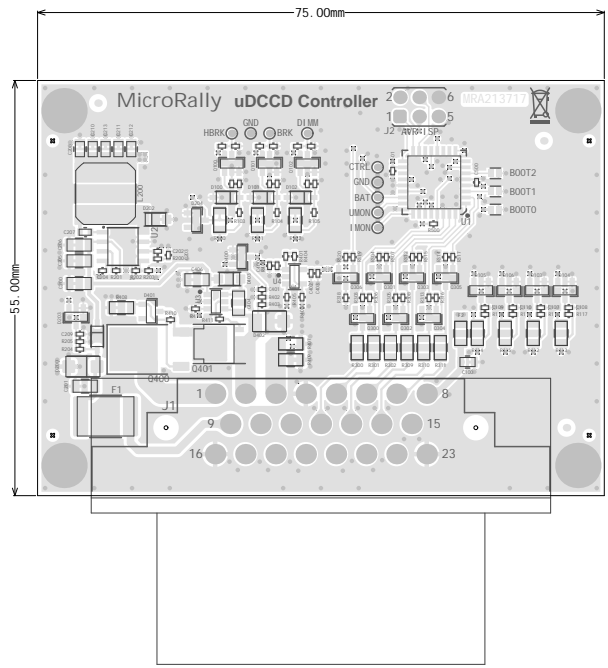
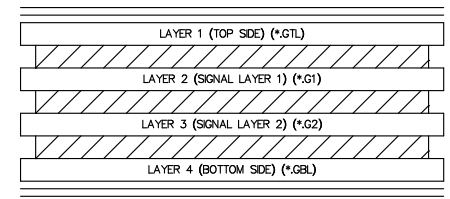


# GERBER NOTES



Symbol	Count	Hole Size	Plated	Hole Type	Via/Pad
✕	337	0.300mm	PTH	Round	Via
⊕	9	0.500mm	PTH	Round	Pad
⊗	6	1.000mm	PTH	Round	Pad
⊗	4	1.152mm	NPTH	Round	Pad
□	23	1.600mm	PTH	Round	Pad
○	2	2.850mm	NPTH	Round	Pad
▽	4	3.600mm	PTH	Round	Pad
	385 Total				

1.0 OZ L1  
 0.20 mm Pregreg - FR4  
 0.5 OZ L2  
 1.065 mm Core - FR4  
 0.5 OZ L3  
 0.20 mm Pregreg - FR4  
 1.0 OZ L4



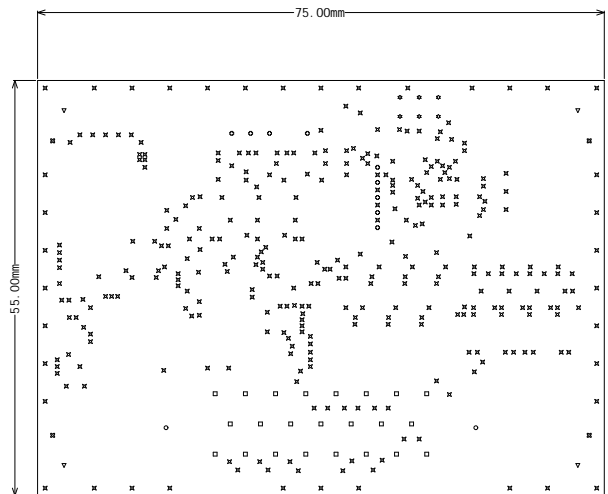
PASTE (TOP SIDE) (\*GTP)  
 SILKSCREEN (TOP SIDE) (\*GTO)  
 SOLDERMASK (TOP SIDE) (\*GTS)  
 1.60 mm +/- 10% LAYER DETAIL 4 LAYERS  
 SOLDERMASK (BOTTOM SIDE) (\*GBS)

## NOTES: (UNLESS OTHERWISE SPECIFIED)

- THIS IS 4 LAYER BOARD
- MATERIAL: FR4, TG 150 DEGREE C MIN
- FR4 DIELECTRIC CONSTANT NOT SPECIFIED
- FINISHED BOARD THICKNESS TO BE 1.60MM +/- 10%
- TRACE WIDTHS IN ARTWORK ARE FINISHED SIZES
- SEE FILM FOR LAYER SEQUENCE AND COPPER THICKNESSES (SHOWN BEFORE PLATING)
- MIN TRACE/SPACE 0.20/0.20MM
- SEE DRILL CHART FOR FINISHED HOLE SIZES
- MIN DRILL 0.30MM
- HOLE TOLERANCE IS +/-3MIL UNLESS OTHERWISE SPECIFIED  
 HOLE COPPER THICKNESS MIN 0.7MIL  
 SLOT TOLERANCE +/-0.1MM  
 BORDER OUTLINE TOLERANCE +/-0.15MM
- SURFACE PLATING: HASL, Pb FREE
- SOLDERMASK: LPI, BOTH SIDES. COLOR GREEN
- SILKSCREEN: TOP SIDE. COLOR WHITE
- ALL BOARDS MUST BE ELECTRICALLY TESTED FOR ISOLATION (SHORTS) AND CONTINUITY (OPENS)

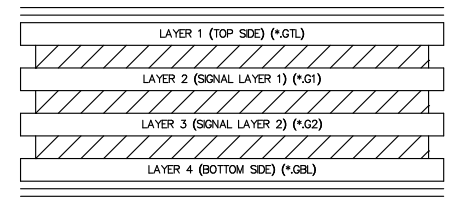
Project: uDCCD Controller	
Author: Andis Jargans	Revision: 7
Date: 15.09.2021	Size: A4
File: uDCCD_controller_r7.PcbDoc	MicroRally

# GERBER NOTES



Symbol	Count	Hole Size	Plated	Hole Type	Via/Pad
✕	337	0.300mm	PTH	Round	Via
⊕	9	0.500mm	PTH	Round	Pad
⊗	6	1.000mm	PTH	Round	Pad
⊗	4	1.152mm	NPTH	Round	Pad
□	23	1.600mm	PTH	Round	Pad
○	2	2.850mm	NPTH	Round	Pad
▽	4	3.600mm	PTH	Round	Pad
	385 Total				

1.0 OZ L1  
 0.20 mm Pregreg - FR4  
 0.5 OZ L2  
 1.065 mm Core - FR4  
 0.5 OZ L3  
 0.20 mm Pregreg - FR4  
 1.0 OZ L4



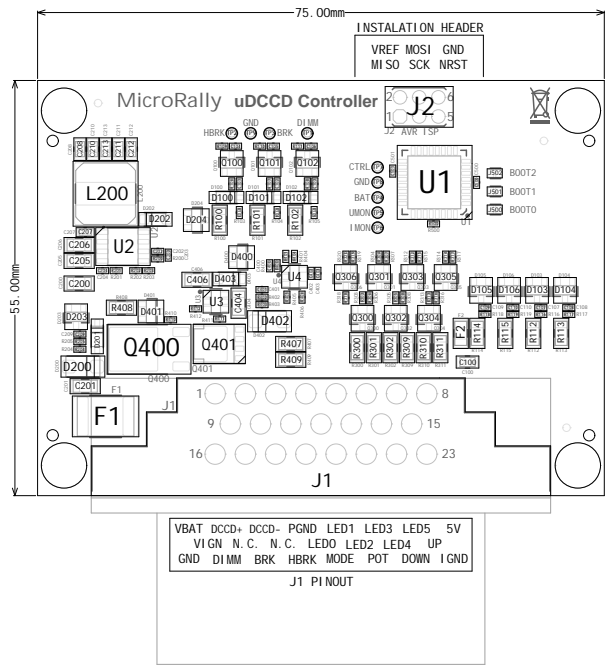
PASTE (TOP SIDE) (\*GTP)  
 SILKSCREEN (TOP SIDE) (\*GTO)  
 SOLDERMASK (TOP SIDE) (\*GTS)  
 1.60 mm +/- 10% LAYER DETAIL 4 LAYERS  
 SOLDERMASK (BOTTOM SIDE) (\*GBS)

## NOTES: (UNLESS OTHERWISE SPECIFIED)

- THIS IS 4 LAYER BOARD
- MATERIAL: FR4, TG 150 DEGREE C MIN
- FR4 DIELECTRIC CONSTANT NOT SPECIFIED
- FINISHED BOARD THICKNESS TO BE 1.60MM +/- 10%
- TRACE WIDTHS IN ARTWORK ARE FINISHED SIZES
- SEE FILM FOR LAYER SEQUENCE AND COPPER THICKNESSES (SHOWN BEFORE PLATING)
- MIN TRACE/SPACE 0.20/0.20MM
- SEE DRILL CHART FOR FINISHED HOLE SIZES
- MIN DRILL 0.30MM
- HOLE TOLERANCE IS +/- 0.3MM UNLESS OTHERWISE SPECIFIED  
 HOLE COPPER THICKNESS MIN 0.7MIL  
 SLOT TOLERANCE +/- 0.1MM  
 BORDER OUTLINE TOLERANCE +/- 0.15MM
- SURFACE PLATING: HASL, Pb FREE
- SOLDERMASK: LPI, BOTH SIDES. COLOR GREEN
- SILKSCREEN: TOP SIDE. COLOR WHITE
- ALL BOARDS MUST BE ELECTRICALLY TESTED FOR ISOLATION (SHORTS) AND CONTINUITY (OPENS)

Project: uDCCD Controller	
Author: Andis Jargans	Revision: 7
Date: 15.09.2021	Size: A4
File: uDCCD_controller_r7.PcbDoc	MicroRally

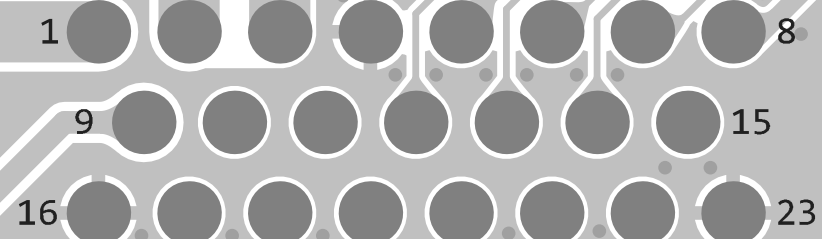
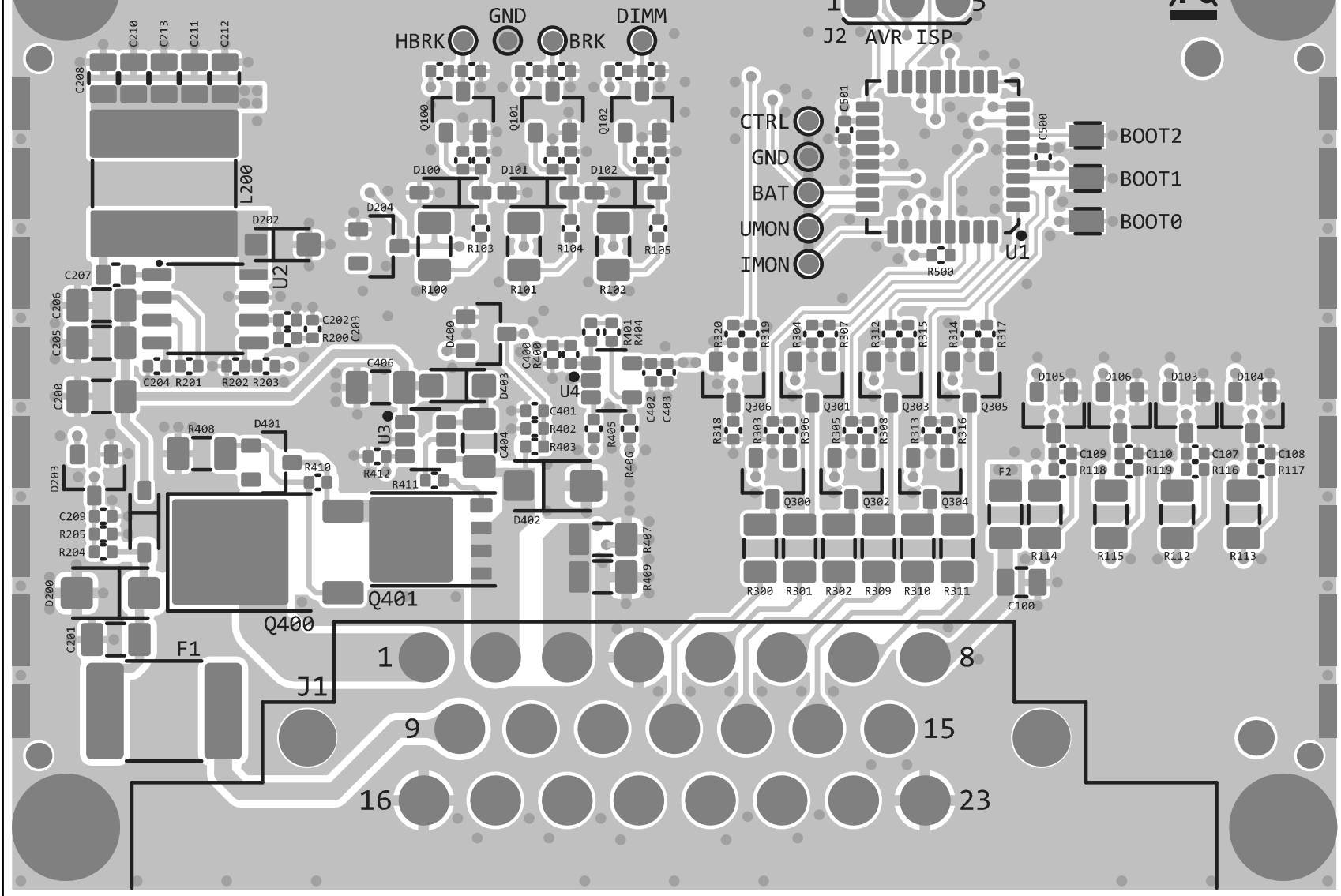
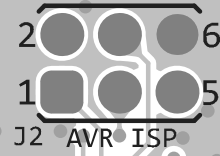
# ASSEMBLY NOTES

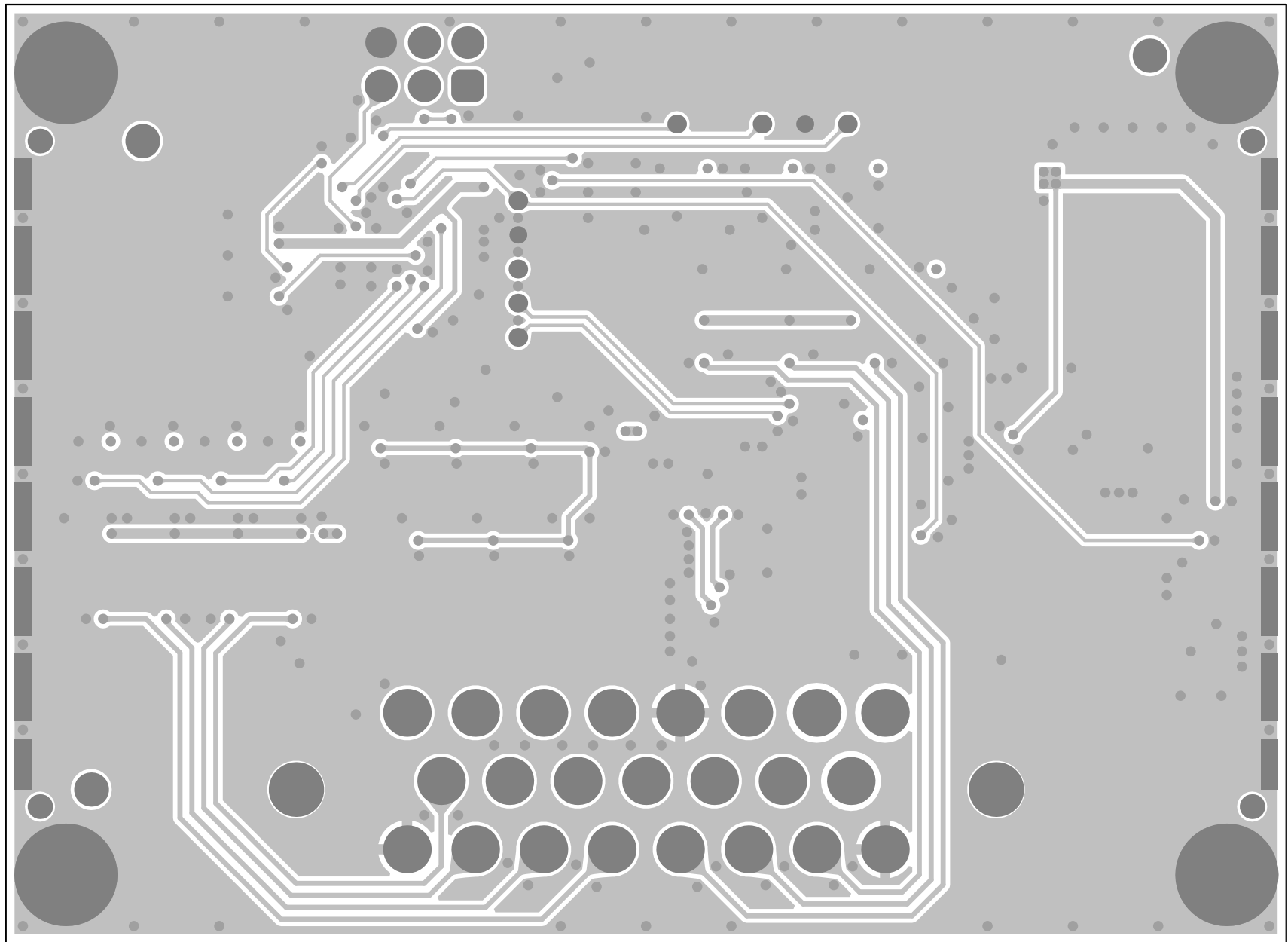


Project: uDCCD Controller	
Author: Andi s Jargans	Revisi on: 7
Date: 15.09.2021	Size: A4
File: uDCCD_control I er_r7.PcbDoc	MicroRally

# MicroRally uDCCD Controller

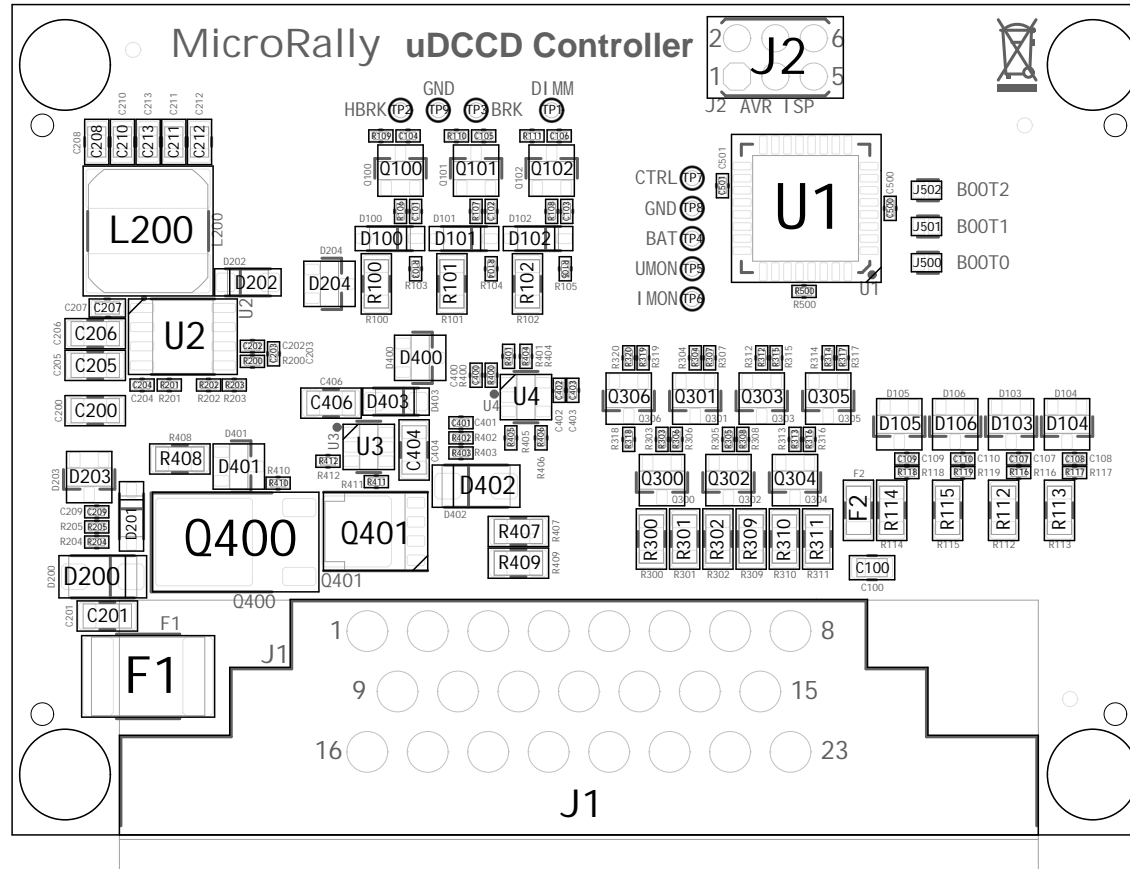
MRA213717





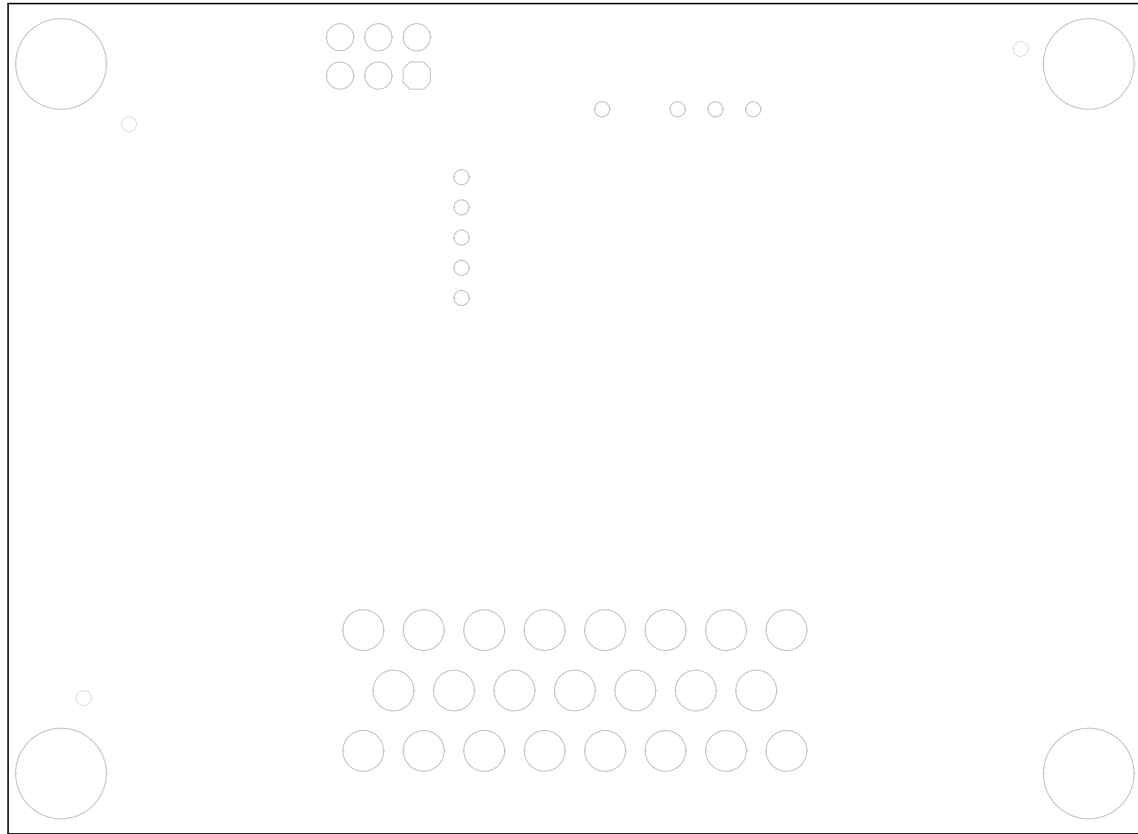
INSTALLATION HEADER

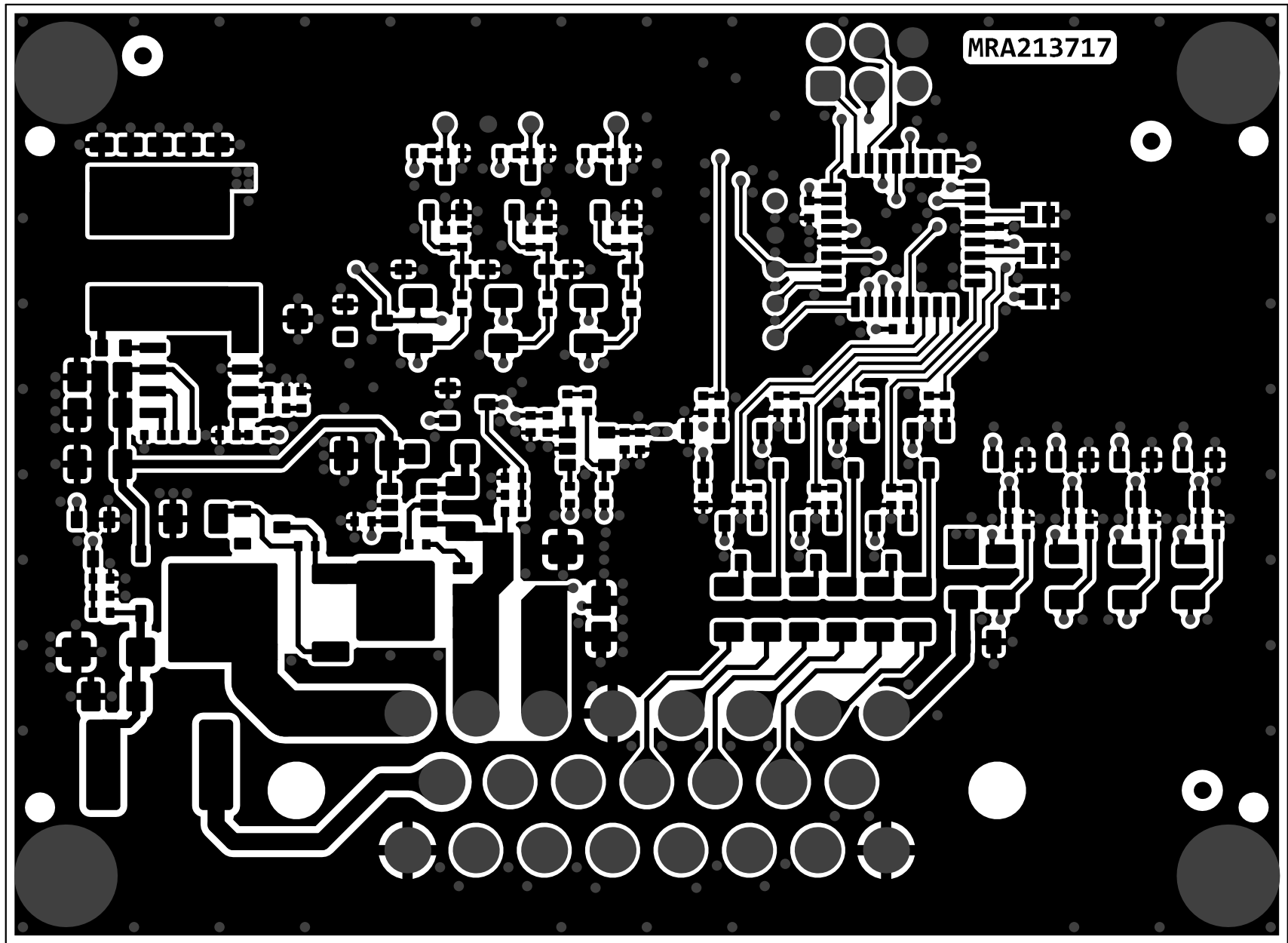
VREF MOSI GND  
MI SO SCK NRST



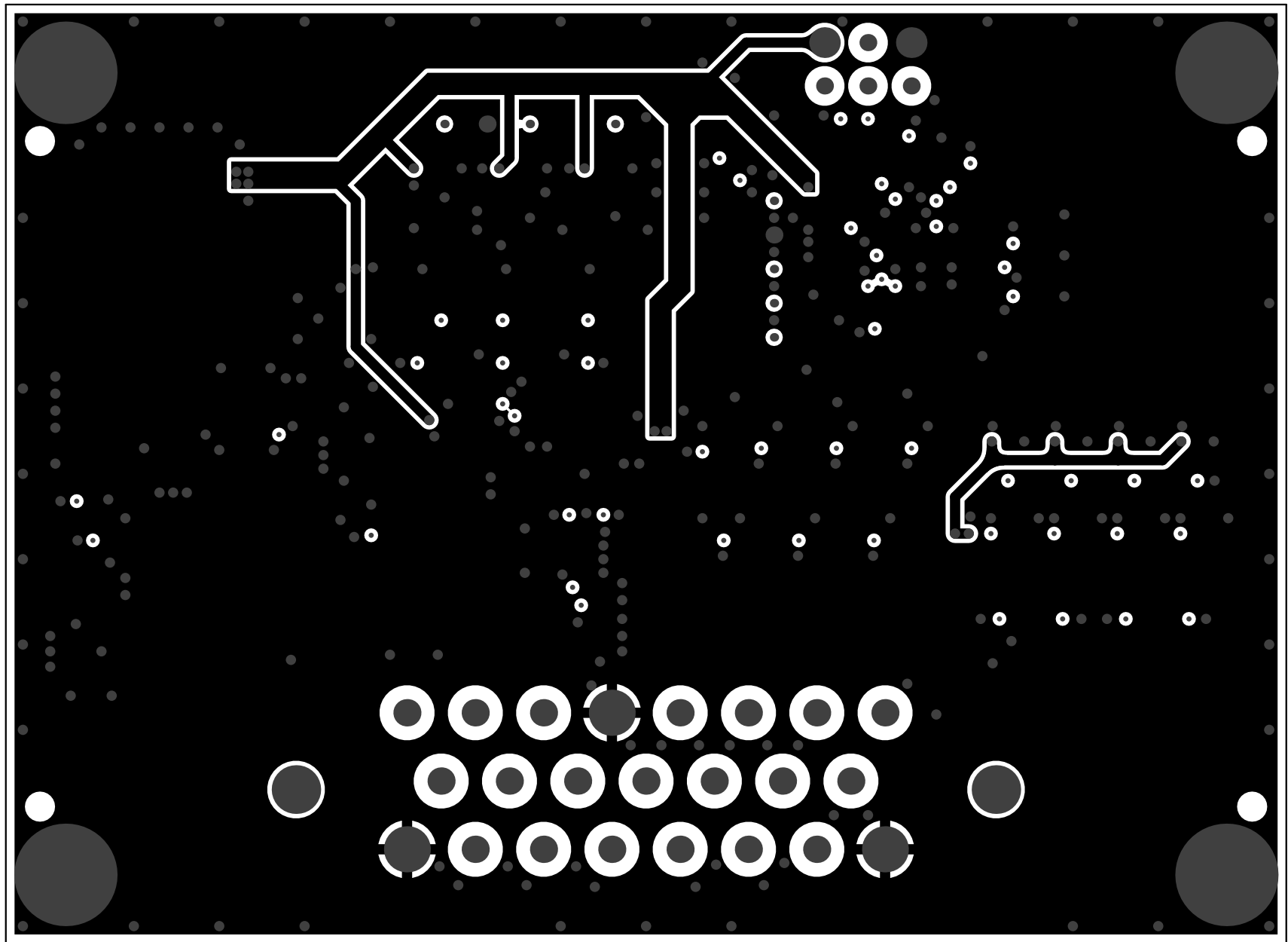
VBAT DCCD+ DCCD- PGND LED1 LED3 LED5 5V  
VIGN N.C. N.C. LED0 LED2 LED4 UP  
GND DIMM BRK HBRK MODE POT DOWN IGND

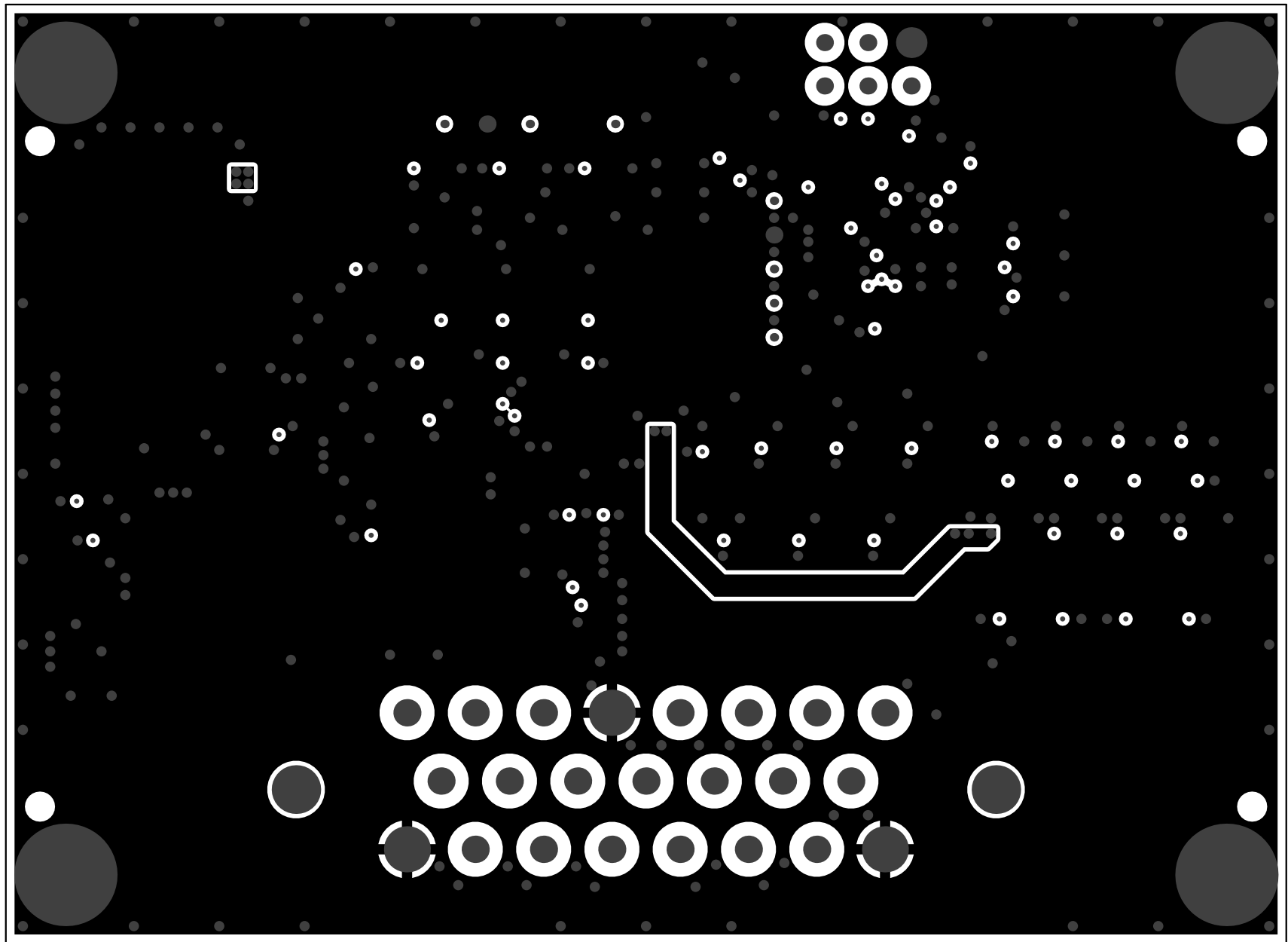
J1 PINOUT

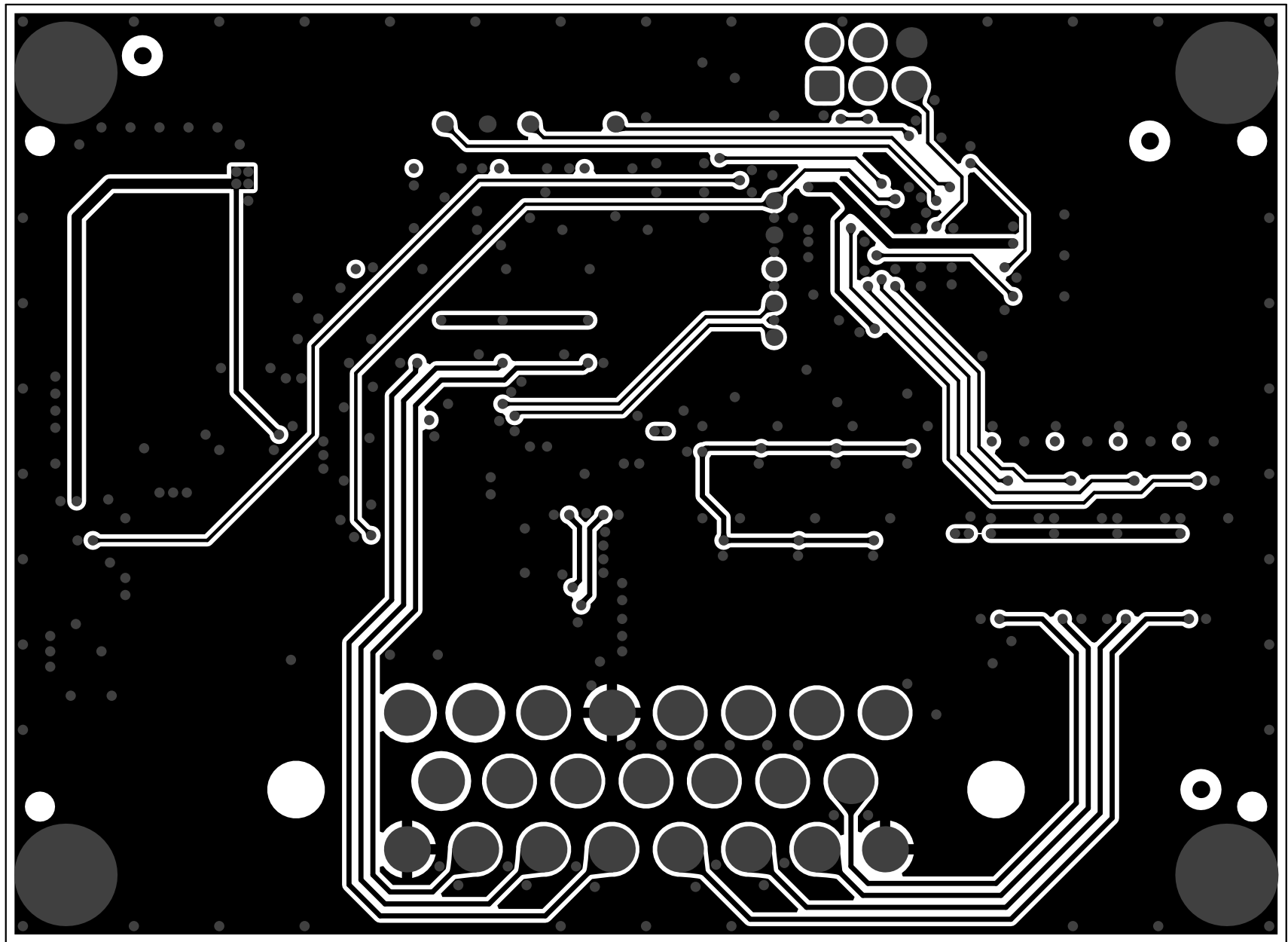




MRA213717







# MicroRally uDCCD Controller

MRA213717

