MicroRally

uDCCD Controller

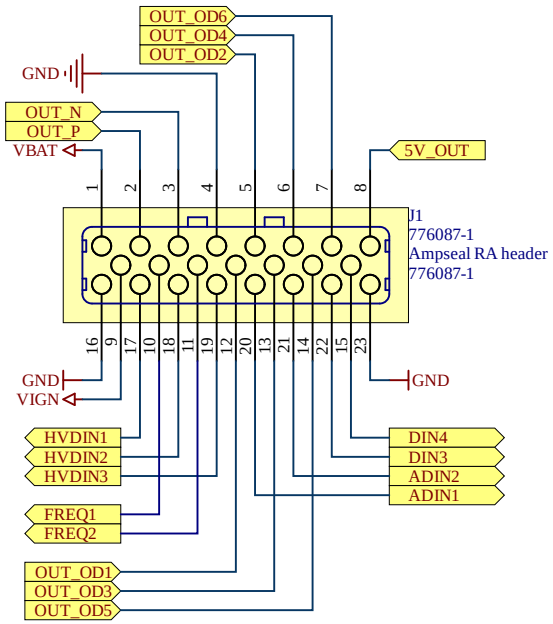
Subaru DCCD Coil controller

PCB Revision R9

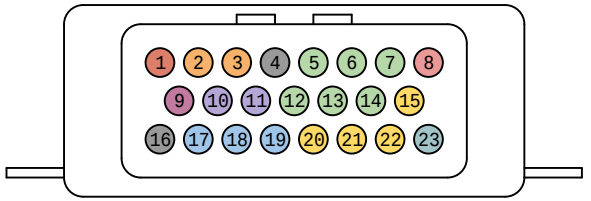
Title: Cover page				MicroRally
Project: uDCCD Controller				
PCB: R9	BOM: V1	Sheet 1 of 12	Size: A4	Engineer: Andis Zīle
File: Cover_page.SchDoc				Date: 10.10.2023

Index

Title: Index				MicroRally
Project: uDCCD Controller				
PCB: R9	BOM: V1	Sheet 2 of 12	Size: A4	Engineer: Andis Zīle
File: Index.SchDoc				Date: 10.10.2023

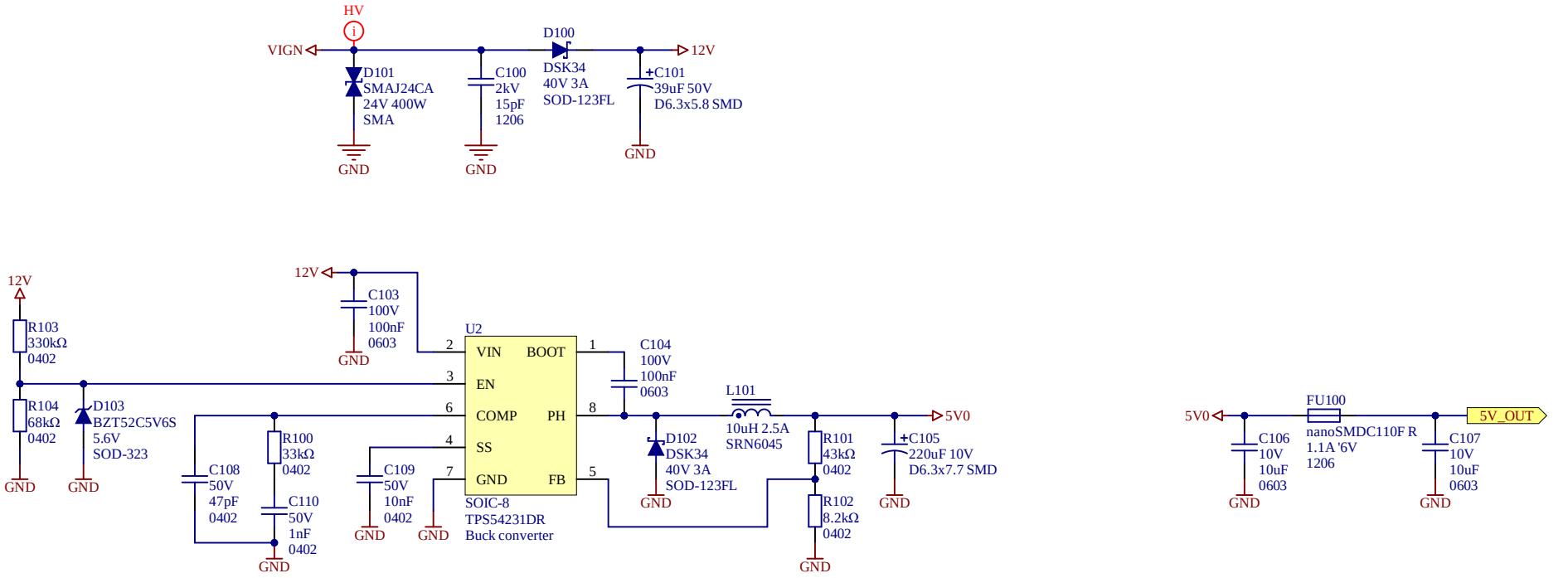


MAIN CONNECTOR

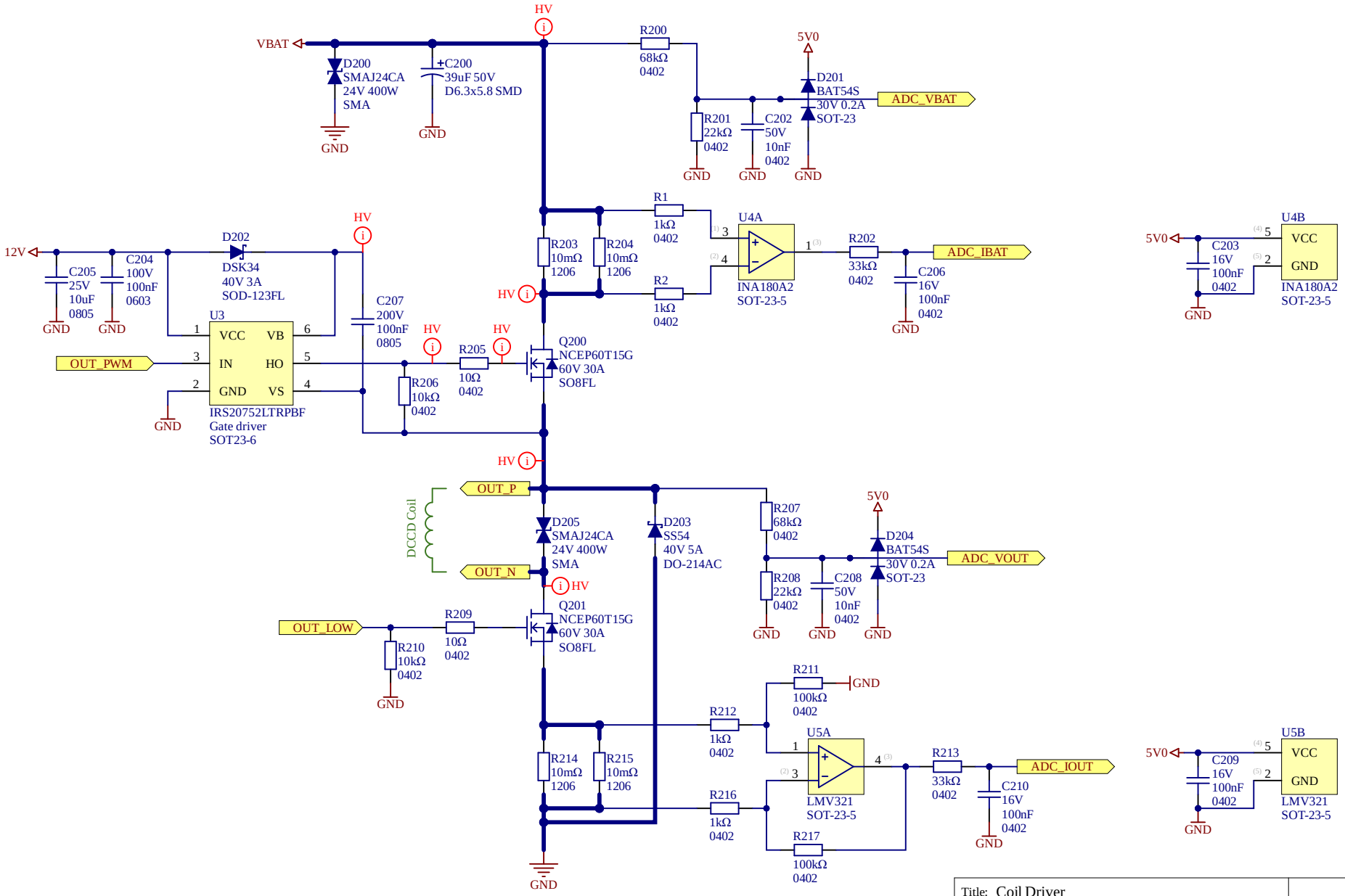


1	VBAT	Coil power supply
2	OUTH	Coil switching supply
3	OUTL	Coil return
4	GND	Power ground
5	OD2	Display 20% output
6	OD4	Display 60% output
7	OD6	Display 100% output
8	5V	5V supply output
9	IGN	Ignition power
10	FREQ1	Front speed input
11	FREQ2	Rear speed input
12	OD1	Display 0% output
13	OD3	Display 40% output
14	OD5	Display 80% output
15	DIN4	Up (+) button input
16	GND	Logic power ground
17	HVDIN1	Display dimm input
18	HVDIN2	Brakes signal input
19	HVDIN3	Handbrake signal input
20	ADIN1	Mode button input / Analog input
21	ADIN2	Potentiometer input / TPS input
22	DIN3	Down (-) button input
23	GND	Inputs ground

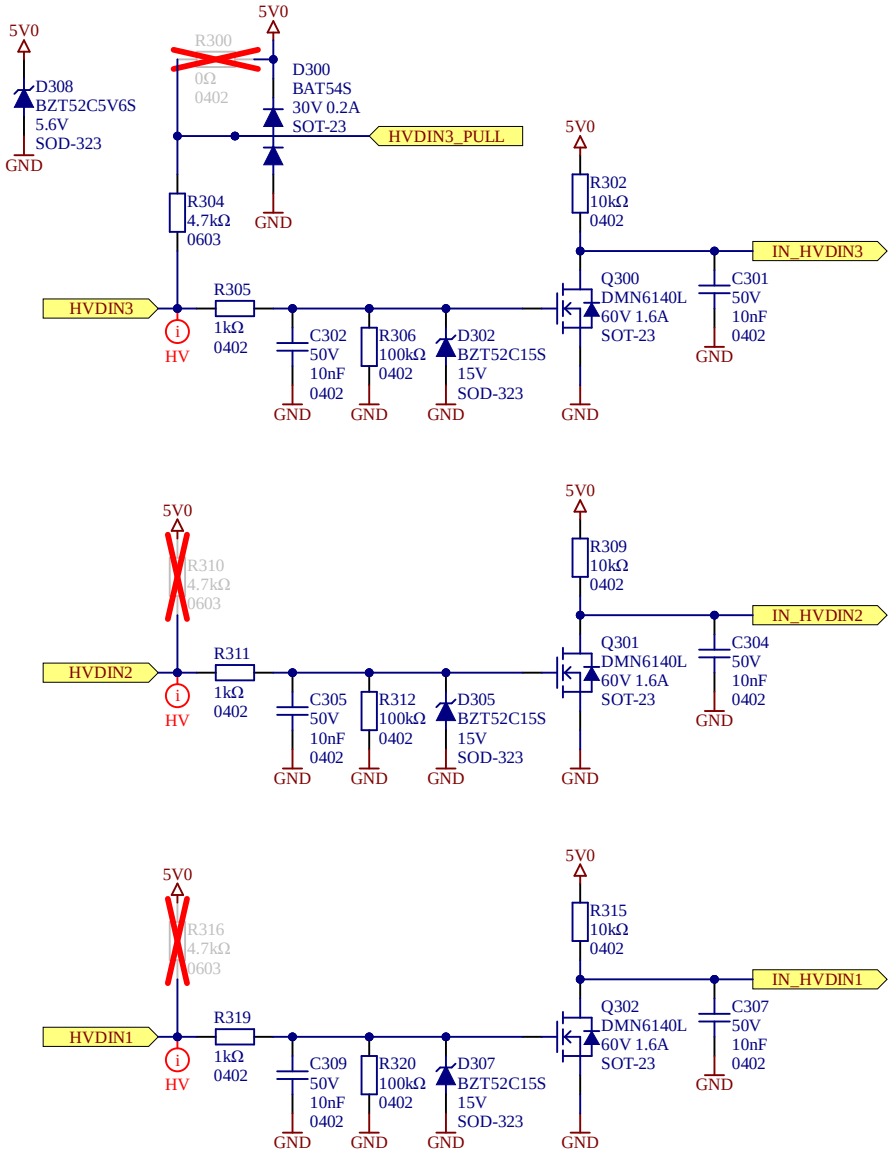
Title: Main connector				MicroRally
Project: uDCCD Controller				
PCB: R9	BOM: V1	Sheet 3 of 12	Size: A4	Engineer: Andis Zīle
File: Main_Connector.SchDoc				Date: 10.10.2023

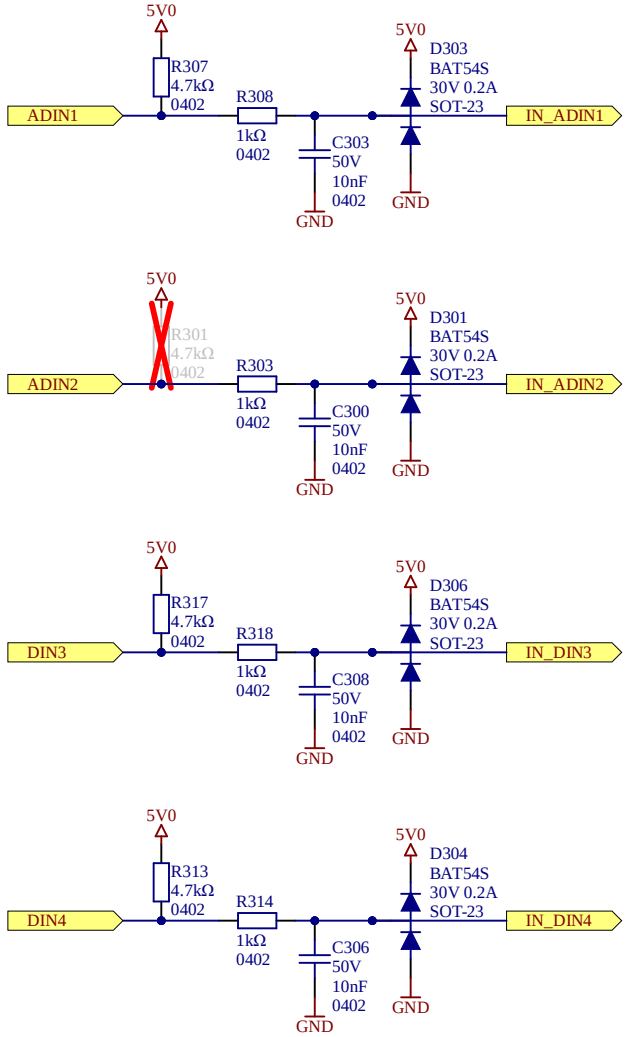


Title: Logic power					MicroRally
Project: uDCCD Controller					
PCB: R9	BOM: V1	Sheet 4 of 12	Size: A4		Engineer: Andis Zīle
File: Power.SchDoc					Date: 10.10.2023

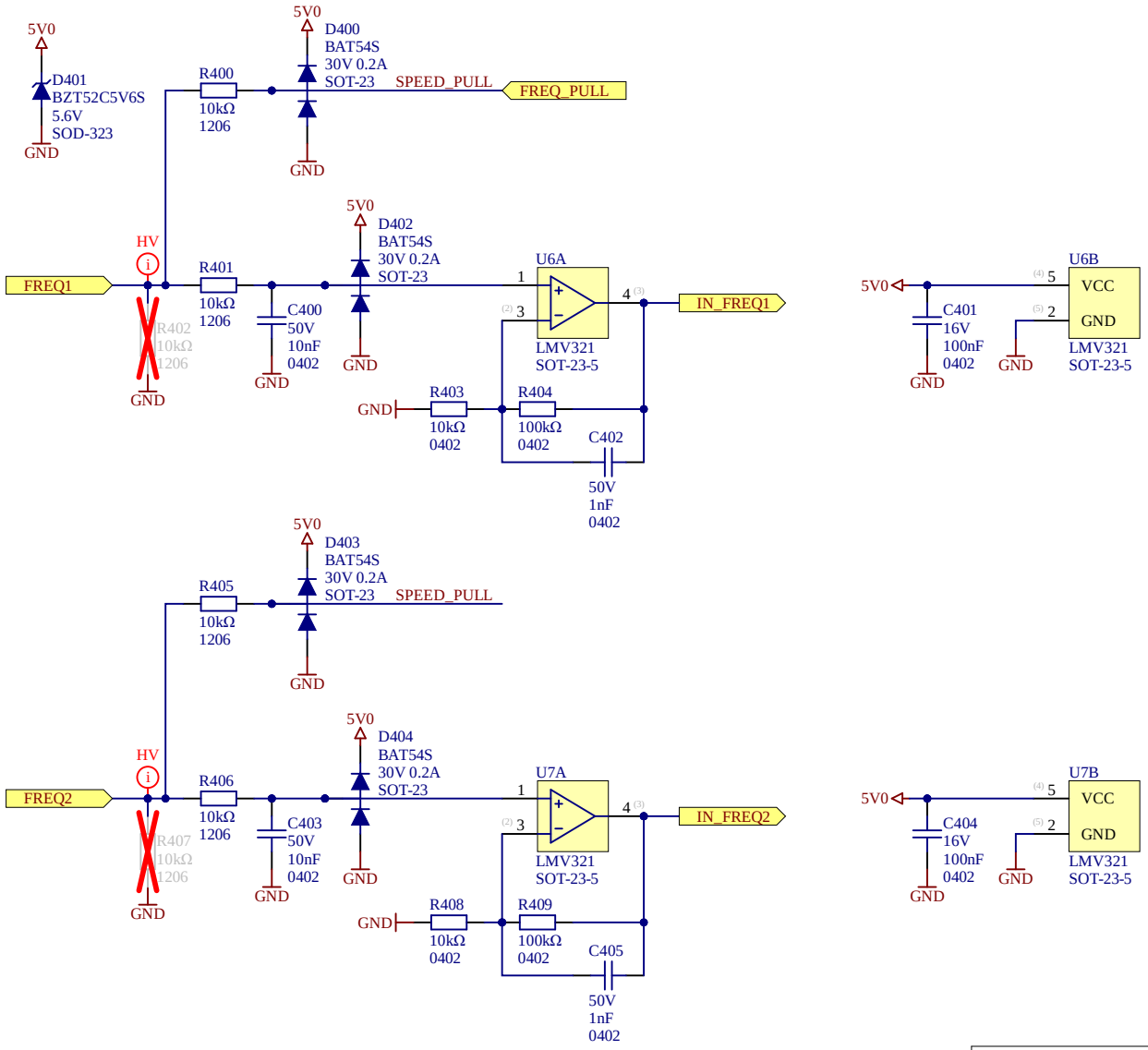


Title: Coil Driver				MicroRally
Project: uDCCD Controller				
PCB: R9	BOM: V1	Sheet 5 of 12	Size: A4	Engineer: Andis Zīle
File: Coil_driver.SchDoc				Date: 10.10.2023

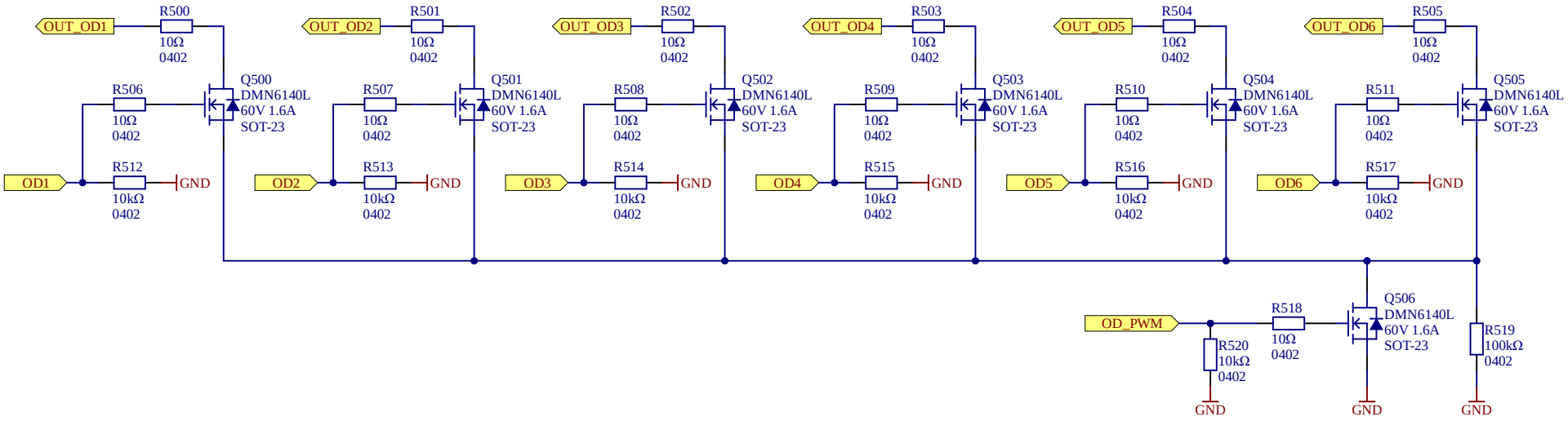




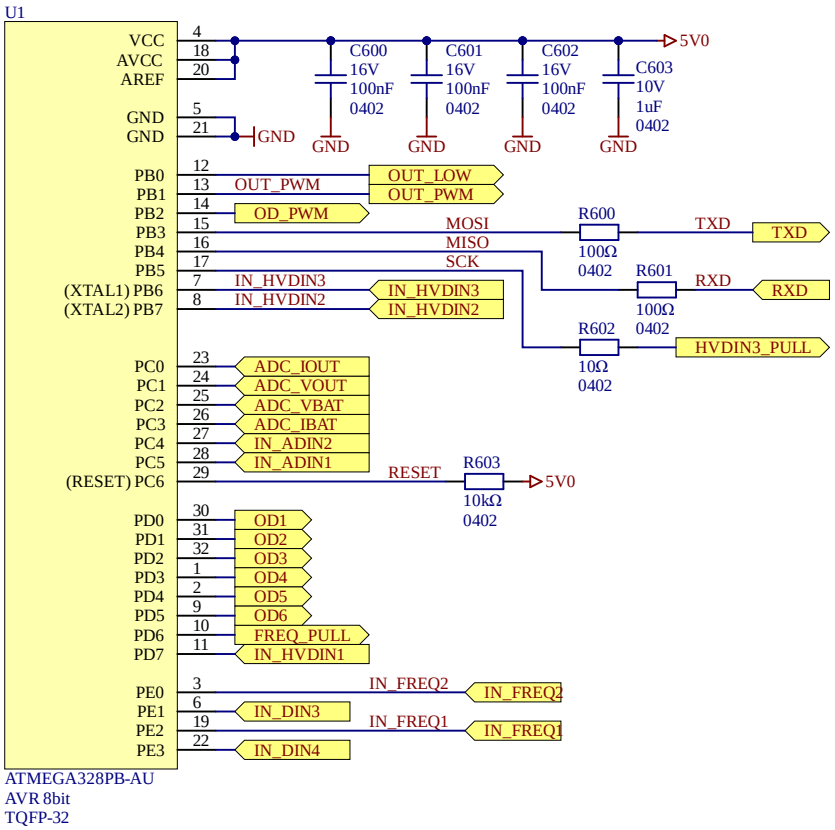
Title: User inputs				MicroRally
Project: uDCCD Controller				
PCB: R9	BOM: V1	Sheet 6 of 12	Size: A4	Engineer: Andis Zīle
File: Chasis_inputs.SchDoc				Date: 10.10.2023



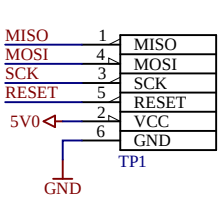
Title: Speed inputs				MicroRally
Project: uDCCD Controller				
PCB: R9	BOM: V1	Sheet 7 of 12	Size: A4	Engineer: Andis Zīle
File: Speed_inputs.SchDoc				Date: 10.10.2023

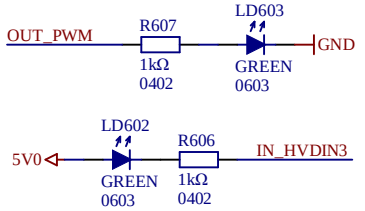


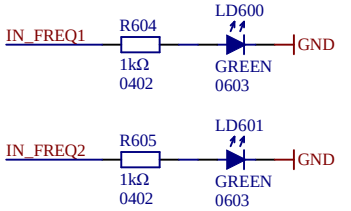
Title: LED Display outputs					MicroRally
Project: uDCCD Controller					
PCB: R9	BOM: V1	Sheet 8 of 12	Size: A4		Engineer: Andis Zīle
File: LEDs.SchDoc					Date: 10.10.2023



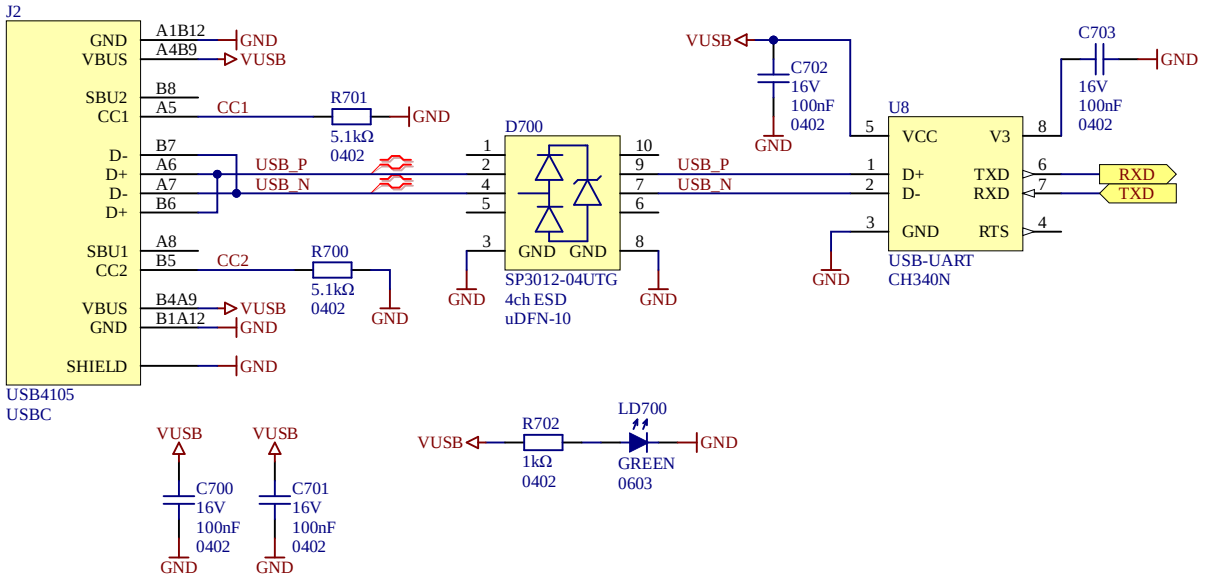
#	Pin	GPIO	Special	Analog	Timer 0 (8b)	Timer 1	Timer 2 (8b)	Timer 3	Timer 4	UART	SPI	I2C	INT		Usage
12	PB0	OUT	CLKO			ICP1									DCCD Enable
13	PB1					OC1A									DCCD PWM
14	PB2					OC1B					SS0				LED PWM
15	PB3						OSC2A			TXD1	MOSI0				ISP / Config UART
16	PB4									RXD1	MISO0				ISP / Config UART
17	PB5	OUT								XCK1	SCK0				ISP / Handbrake pull-up
7	PB6	IN	XTAL1 / TOSC1												HBRAKE
8	PB7	IN	XTAL2 / TOSC2												BRAKE
23	PC0			ADC0							MISO1				DCCD Current
24	PC1			ADC1							SCK1				DCCD Voltage
25	PC2			ADC2											Batery voltage
26	PC3			ADC3											Battery current
27	PC4			ADC4								SDA0			Potentiometer / TPS
28	PC5			ADC5								SCL0			MODE Button
29	PC6		RESET												Reset & ISP
30	PD0	OUT						OC3A		RXD0					DSP0
31	PD1	OUT							OC4A	TXD0					DSP1
32	PD2	OUT						OC3B	OC4B				INT0		DSP2
1	PD3	OUT					OC2B						INT1		DSP3
2	PD4	OUT			T0					XCK0					DSP4
9	PD5	OUT			OC0B	T1									DSP5
10	PD6	IN		AIN0	OC0A										Speed pull-up
11	PD7	IN		AIN1											DIMM IN
3	PE0			ACO					ICP4			SDA1			Speed input 2
6	PE1	IN							T4			SCL1			DOWN Button
19	PE2			ADC6				ICP3			SS1				Speed input 1
22	PE3	IN		ADC7				T3			MOSI1				UP Button







Title: Controller			MicroRally
Project: uDCCD Controller			
PCB: R9	BOM: V1	Sheet 9 of 12 Size: A4	Engineer: *
File: Controller.SchDoc			Date: 10.10.2023



Title: Main connector					MicroRally
Project: uDCCD Controller					
PCB: R9	BOM: V1	Sheet 10 of 12	Size: A4		Engineer: Andis Zīle
File: USB.SchDoc					Date: 10.10.2023

PCB Sheet
H1

4 Layer Stackup
H2

PCB DM
H3

WEEE
H4

MH1
GND
M3 D3.2

MH2
GND
M3 D3.2

MH3
GND
M3 D3.2

MH4
GND
M3 D3.2

FI1
FI2
FI3
FI4

TH1
TH2
TH3
TH4

Title: Miscellaneous				MicroRally
Project: uDCCD Controller				
PCB: R9	BOM: V1	Sheet 11 of 12	Size: A4	Engineer: Andis Zīle
File: Miscellaneous.SchDoc				Date: 10.10.2023

Revision history

PCB	BOM	Date	Fixed issue	Changes
R6	V1	2020-08-05		Initial design.
R7	V1	2021-02-23	MiniFit connecotrs aren't serious.	Changed to TE Ampseal connector
		2021-03-05	Handbrake input doens't work reliably.	HV inputs changed to HiZ type. Q100-Q102 changed to N-ch MOSFETs.
		2021-03-17	No support for JLC Assembly process.	Added JLC PCB SMT assembly tooling holes.
		2021-06-10		Added block diagram and miscellaneous page
		2021-09-15	Time constant of DCCD voltage and currnet LPF should be the same.	Voltage and currnet monitor LFP values changed to have equal time constants.
		2021-09-23	Can't precisely regulate output voltage if there is drop in supply wires.	Supply volatge monitor connected to VBAT. Added load option to measure Ignition supply.
R8	V1	2023-06-02	Chip supply issues	Changed MCU to ATmega328PB
			Need optional speed axis speed inputs	Added VR/HALL speed inputs to previsoly not connected pins.
			Need more software defined configuration	Added GPIO controller pull-ups.
			Need PC interface to change configuration.	Added USB-UART interface.
			Can't reliably detect fusing current	Added high side current monitor
			Can't turn off DCCD in short-to-high situation.	Added low side switch. Also option for fast coil decay during handbrake pull.
R9	V1	2023-09-21	Coil current sense via has short to "real" ground	Added polygon cutout
				Other minor layout improvements
		2023-10-10		Renamed signals to aplication agnostic naming

Title: Revision history				MicroRally
Project: uDCCD Controller				
PCB: R9	BOM: V1	Sheet 12 of 12	Size: A4	Engineer: Andis Zīle
File: History.SchDoc				Date: 10.10.2023